Fabrication of a micro-lens array for Reflective Electron Beam Lithography

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1. Introduction
This paper describes the fabrication process of an electrostatic micro-lens (lenslet) array for the Reflective Electron Beam Lithography (REBL) tool [1,2]. The REBL concept is designed to enable a high throughput e-beam writing process for maskless lithography. The lenslet array is a key component in the set-up. It enables the splitting of a single incoming e-beam into an array of beamlets that can be controlled individually.

![Fig 1. A tilted XSEM view of the lenslet structure and a cross section view with an illustration of the electron beam reflection principle](image)

The lenslet structure has to be covered (fig 3) with a high resistive coating layer to prevent charge build-up[3] on the sidewalls. The coating needs to be in contact with all electrode layers. Therefore, the different electrode layers are exposed with slightly different hole diameters (Table I) and stringent alignment requirements have to be met.

Table1: litho performance: hole diameter, applied overlay corrections to underlying electrode and overlay performance after corrections.

<table>
<thead>
<tr>
<th>Ring elecr.</th>
<th>Mask CD (nm)</th>
<th>litho CD (nm)</th>
<th>Overlay corr. X (nm)</th>
<th>Overlay mean X (nm)</th>
<th>Overlay 3σ X (nm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Top</td>
<td>1440</td>
<td>1359</td>
<td>13.4</td>
<td>0.2</td>
<td>17.1</td>
</tr>
<tr>
<td>Upper</td>
<td>1380</td>
<td>1311</td>
<td>-15.2</td>
<td>-11.7</td>
<td>10.9</td>
</tr>
<tr>
<td>Middle</td>
<td>1340</td>
<td>1267</td>
<td>-20.0</td>
<td>-8.0</td>
<td>14.5</td>
</tr>
<tr>
<td>Lower</td>
<td>1300</td>
<td>1220</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
</tr>
</tbody>
</table>

Overlay measurements show that shifts (translational)
from layer to layer in the order of 10 to 50nm (mean value) are present. These mismatches can be reduced by implementing an overlay feedback loop. The table I shows the applied corrections and remaining overlay errors.

In parallel to the hole patterning development, a study was carried out to find a suitable high resistive coating. The best candidate film was an ALD TiAlO film. Both the Ti to Al ratio and the film thickness (fig 3) are tuned to achieve a film with the sheet resistance values in the targeted range (TΩ/ ) and a stable behavior for the voltage range from 0.01 to 0.3MV/cm.

![Image](50x269 to 249x383)

Fig 3: Sheet resistance of the TiAlO film designed as charge drain layer for the lenses

2. Interconnect processing

This section describes the processing required to fabricate the electrical connectivity between the lenslet electrode layers and towards the underlying CMOS chip. To minimize the influence of the interconnects, vias and pads on the lenslet processing a design as depicted in figure 4 was selected.

![Image](129x169 to 255x265)

Fig 4: Schematic and real xsem views of the lenslets with connection to CMOS and the via connections in the pad area

The connections between the various electrode layers is made by arrays of vias (Φ=400nm, aspect ratio 2). The vias are filled by the electrode TiN deposition only. To achieve sufficient sidewall coverage inside the via, a combination of ALD and PVD TiN is used. The ALD layer provides sidewall coverage in the vias for improved conductivity while the PVD layer is used to reach the target thickness of 60nm for the electrode layer (Fig. 4).

The resistance of a single via is measured to be less than 1kΩ. Multiple vias are placed in parallel to obtain resistance values of less than 10Ω for the interconnects between the top and bottom electrode layers.

For the connections to the CMOS circuit a resistance of less than 0.2Ω is required in the bondpads. This is achieved by placing the Al layer from the bonding pads immediately on top of the bottom electrode. This design avoids using the complexity of additional low resistive layers (Cu or Al) between the lenslet via and electrode levels. The bottom electrode of each hole is connected directly to the Metal9 Cu level of the CMOS DPG chip. This was achieved by patterning a 900nm wide via through the 150nm capping layer on top of the metal9.

The full functionality of the chip can only be fully demonstrated in the REBL e-beam column after mounting and the chip on special purpose package. So far a static testchip (without the CMOS) was mounted successfully in the ebeam column for demonstration of the lenslet focusing behavior. First line patterns were generated with this set-up[4].

3 Conclusions

This paper describes a novel process for the production of electrostatic lenslets for the REBL tool. We have shown the patterning of the lenslet structures with good control over hole diameter, uniformity and alignment and integrated the device on top of a CMOS DPG chip with all required electrical connections. Work is ongoing to prove the full device performance in the REBL tool.

Acknowledgements

This work is supported by DARPA1 and KLA-Tencor under the DARPA Agreement No. HR0011-07-9-0007. The authors wish to thank J.Swerts and M. Popovici for development of the ALD layer.

References


1 The views, opinions, and/or findings contained in this article are those of the author and should not be interpreted as representing the official views or policies, either expressed or implied, of the Defense Advanced Research Projects Agency or the Department of Defense.