

Light Detection and Emission in Germanium-On-Insulator Diodes

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1. Introduction

In Si photonics, Ge is a promising material for achieving monolithic integration of photo-diodes (PDs) [1, 2] and light emitters [3, 4] on a Si chip, because its high absorption coefficient in the near-infrared region is critical for PDs, and its pseudo-direct band gap character is suitable for light emitters. Direct epitaxial growth of Ge on Si is one of the most promising approaches for fabricating Ge PDs and light emitters. Accordingly, high performance Ge PDs with a 3-dB bandwidth of 49 GHz [2] and optically pumped lasing [4] have been demonstrated. However, the direct growth of Ge on Si induces huge amounts of defects at the Ge/Si interface owing to the lattice constant mismatch of 4 %. The complex nature of the Ge/Si interface makes it difficult to identify the exact origin of defects and subsequent large dark currents. Another approach for the Ge integration is to use germanium-on-insulator (GeOI) substrates made by the wafer bonding technique [5]. In this case, a relaxed Ge layer grown on a graded SiGe buffer layer can be used. Nevertheless, the use of GeOI substrates in the standard complementary metal oxide semiconductor (CMOS) production line is difficult, and several issues such as contamination, surface cleaning, thermal stability must be addressed. In this work, to highlight the challenges facing introduction of GeOI *pin* diodes, we fabricated lateral GeOI *pin* diodes by standard CMOS processes for the first time. To understand their basic transport and optical properties, we then characterized them as PDs and light emitters.

2. Device structure and fabrication process

Figure 1 shows the schematic structures and the equivalent circuit of the lateral GeOI *pin* diodes with interdigitated comb electrodes. Here, W and S represent the width and the space of the electrodes, respectively. The GeOI diodes were fabricated on 8-inch GeOI wafers with GeOI thickness of 80 nm and buried oxide (BOX) thickness of 140 nm. The initial dislocation density of the GeOI layer was about $10^7/\text{cm}^2$. After surface cleaning by diluted HF solution, SiO_2 with a thickness of 25 nm was deposited at 400 °C to avoid the evaporation of GeO expected at temperatures higher than 425 °C in air [6]. Then, 15-nm-thick Si_3N_4 was deposited on the SiO_2 as a hard mask for contact holes. After that, *p*-type and *n*-type diffusion regions were formed by ion implantation. The impurities were activated in N_2 atmosphere. Si_3N_4 was patterned by reactive ion etching and SiO_2 was partially removed by HF solution to

make contact holes. Lastly, TiN and Al were sputtered and patterned as metal interconnects.

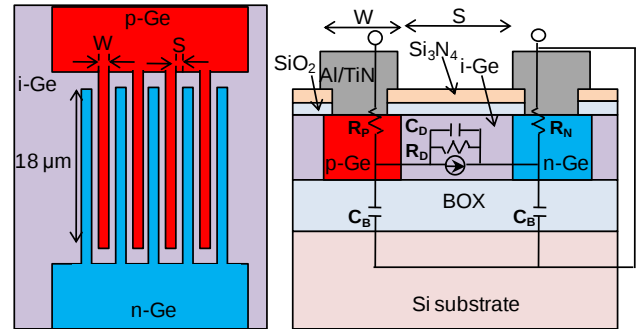


Fig. 1 Schematic structures of GeOI diodes. (a) Plain view of GeOI diodes. (b) Cross-sectional view and equivalent circuit model of GeOI diodes.

2. Results and Discussion

Electrical characterization

Table 1 summarizes the electrical properties of the *p*-type, *n*-type, and intrinsic regions of the GeOI layer at room temperatures. The carrier density of the *p*-type and *n*-type GeOI in the order $10^{18}/\text{cm}^3$ was reduced more than one order of magnitude compared with the expected carrier density presumably because of the out-diffusion of impurities in the N_2 annealing after ion implantation. The carrier density in the intrinsic GeOI was estimated to be about $10^{17}/\text{cm}^3$ from sheet resistance $R_{\square}$. In fact, the Hall voltage in the intrinsic GeOI was almost zero, suggesting there are comparable amounts of holes and electrons in the intrinsic GeOI. The contact resistivity at the TiN/Ge interfaces is higher in the *n*-type region than that in the *p*-type GeOI owing to the Fermi-level pinning caused by the surface states near the valence band [7].

Table 1 Electrical properties of *p*-type, *n*-type, and intrinsic GeOI layer.

	$R_{\square}[\text{k}\Omega]$	Carrier density $[\text{cm}^{-3}]$	Mobility $[\text{cm}^2/\text{Vs}]$	$\rho_c[\Omega\text{cm}^2]$
<i>p</i> -type	0.784	6.8×10^{18}	150	2.1×10^{-4}
intrinsic	29.47	$\sim 10^{17}$	—	—
<i>n</i> -type	1.609	1.7×10^{18}	250	3.1×10^{-3}

Photosensitivity and RF response

Figure 2(a) shows photo-currents and dark currents of GeOI diodes with $W=2000$ nm and $S=500$ nm, respectively. An excitation light with wavelength of 1550 nm and power of 12.5 mW was injected vertically into the substrate. Photosensitivity was 1.56 $\mu\text{A}/\text{mW}$ at reverse bias voltage of 1

V. This low sensitivity is mainly due to the thin GeOI layer of 80 nm. In consideration of the effective area and the reflection at the surface, the absorption coefficient α of GeOI layer is calculated as 1524 cm^{-1} , which is comparable to the value in bulk Ge. The photosensitivity can be improved by using a thicker GeOI layer and anti-reflection coating. Dark current density is 6.38 A/cm^2 at reverse bias voltage of 1 V (Fig. 2 (a)). Dark current is generated from defects such as interface traps and threading dislocations. The dark current in the GeOI diode is comparable to those in the reference Si diode fabricated by exactly the same processes. We therefore think that the direct SiO_2 deposition after the surface cleaning induced the large amounts of interface traps at the interface. In fact, thermal oxidation is usually employed to passivate the Si surface, and it would be required to establish similar passivation processes for GeOI.

Figure 2(b) shows the radio frequency (RF) response of the GeOI diodes at reverse bias voltages of 3 V and 10V, respectively. The 3-dB bandwidth at each bias voltage is about 2 GHz, which suggests the RF response of GeOI diodes is limited by the product of resistance and capacitance of the diodes. RF response was analyzed on the basis of the equivalent circuit shown in Fig. 1(b). The simulation results agree with the experimental results without any fitting parameters. According to this model, the 3-dB bandwidth is severely limited by the contact resistances of the *p*-type and *n*-type electrodes and it can be improved up to 30 GHz by sufficiently reducing the contact resistivity.

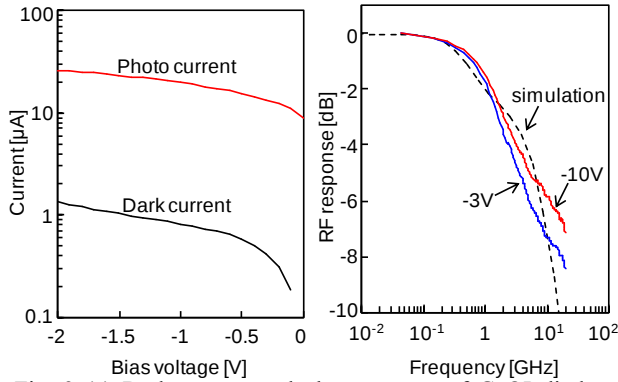


Fig. 2 (a) Dark current and photo current of GeOI diodes with $W=2000\text{nm}$ and $S=500\text{nm}$. (b) Frequency response of GeOI diodes with $S=300\text{nm}$ and $W=900\text{nm}$ at wavelength of 1550nm. Dotted line is obtained by simulation.

Photo-luminescence and electro luminescence

Figure 3(a) shows the photo-luminescence (PL) spectra of *p*-type, *n*-type, and intrinsic regions of the GeOI layer excited by Ar ion laser with wavelength of 458 nm and pump power of 150 mW. All PL spectra show peak wavelengths near 1600 nm. The peak wavelengths are longer than the wavelength of the direct transition of 1550 nm in bulk Ge. The red-shifts of the peak wavelength are thought to be caused by the biaxial tensile strain of 0.2% induced by the difference between thermal expansion coefficients of Ge and SiO_2 [8]. The PL intensity in *n*-type GeOI region is higher than those in intrinsic and *p*-type GeOI regions. This is because the *n*-type doping increases the direct recombi-

nation in Ge by filling the indirect L valleys and populating the direct Γ valley with electrons [9].

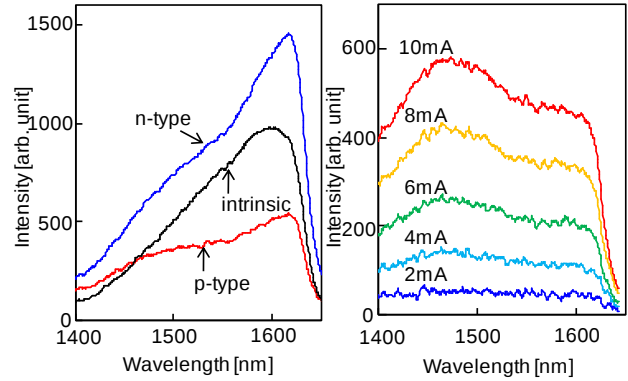


Fig. 3 (a) PL spectra of *p*-type, *n*-type, and intrinsic GeOI. (b) EL spectra of GeOI diodes for several injection currents.

Figure 3(b) shows the electro-luminescence (EL) spectra of the GeOI diodes obtained by forward current injections. The peak wavelengths of the broad EL spectra are near 1460 nm, which is shorter than those observed in PL. The difference between the PL and EL spectra is thought to be originated from the excited region in the GeOI. It is clear from the EL measurements that the current paths are probably dominant at the surface because of the large amounts of interface traps. It is thought that the EL peaks came from the Si-Ge bonds formed by the inter-diffusion of Ge and sub-oxide SiO_{2-x} at the interface. It is shown by the PL measurements that the entire GeOI layer is excited. Appropriate surface passivation is therefore considered to be important for improving the efficiency of light-emissions from Ge.

4. Conclusions

We made lateral GeOI *pin* diodes by standard CMOS processes to identify the key challenges facing fabrication of monolithic PDs and light emitters on a Si chip. These diodes were operated as PDs with 3-dB bandwidth of 2 GHz, which is expected to be improved by reducing contact resistance. By applying a forward bias to the diode, EL spectra with peaks at shorter wavelengths than those of PL spectra were obtained. We think these results inferred that the appropriate surface passivation of Ge is critical to enhance the light-emission efficiency.

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References

- [1] S. Luryi, *et al.*, IEEE Trans. Electron. Devices **31**, 1135 (1984).
- [2] S. Klinger, *et al.*, IEEE Photon. Technol. Lett. **21**, 920 (2009).
- [3] J. Menéndez, *et al.*, Appl. Phys. Lett. **85**, 1175 (2004).
- [4] J. Liu, *et al.*, Opt. Lett. **35**, 679 (2010).
- [5] L. Chen, *et al.*, Opt. Express **16**, 11513 (2008).
- [6] K. Prabhakaran, *et al.*, Thin Solid Films **369**, 289 (2000).
- [7] W. Brattain, and J. Bardeen, Phys. Rev. **74**, 231 (1948).
- [8] Y. Ishikawa, *et al.*, Appl. Phys. Lett. **82**, 2044 (2003).
- [9] J. Liu, *et al.*, Opt. Express **15**, 11272 (2007).