Extended Abstracts of the 2011 International Conference on Solid State Devices and Materials, Nagoya, 2011, pp1197-1198

Mobility Difference in Top and Bottom Surfaces of Multilayer Graphene Placed on Silicon Dioxide

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1. Introduction

Graphene, a two-dimensional honeycomb lattice of carbon atoms, has attracted much attention as a promising candidate for the nanoelectronics material. This is mainly owing to its mobility as high as ~200,000 cm^2/Vs [1]. However, it is noted that such excellent mobility can be achieved only in graphene films which are suspended between the source and drain electrodes, and only after a special treatment, called "current annealing"[1]. In conventional graphene devices placed on a Si/SiO_2 substrate, on the other hand, the mobility is limited to ~10,000 cm^2/Vs[2]. Since the construction of graphene electronics with suspended components seems to be unrealistic, to unlock the full potential of this novel material, one needs to examine what is the main factor in deterorating the mobility of graphene placed on a substrate and how one can improve it.

It is known that charged impurities on the surface of graphene films, rather than defects in the graphene lattice, is the main cause of the low mobility in graphene flakes obtained by the mechanical exfoliation [3]. There are several origins for charged impurities in graphene films; charges inside the silicon dioxide of the substrate, to which the bottom surface of the graphene films faces, the adsorbed molecules and contaminations due to chemicals (resist residues and so on) attached to the top surface of graphene. It is not clear which influences more strongly on the mobility of graphene.

This paper aims to evaluate the influence of the impurities on the top and bottom surfaces separately. For this purpose, we use dual-gated multilayer graphene with a contactless top gate. We develop a method to estimate the mobility of the top and bottom surfaces of *multilayer* graphene (MLG).

2. Experiment

We fabricated dual-gated graphene devices with a *contactless* top gate using the conventional technique[4]. A scanning electron microscopy (SEM) image of a sample is shown in Fig. 1. Here, a Ti top gate, which does not contact with the MLG, and Au/Pd electrodes for four-terminal measurement are attached to the MLG. The highly-doped Si/SiO_2 substrate was used as the back gate. The MLG films, which were obtained by the mechanical exfoliation of kish graphite [5], have thickness of 1.0 – 2.4 nm. No annealing was carried out for the MLG flakes. The conductance of the MLG was calculated from the current-voltage characteristics below the bias of 1 mV measured in vacuum (~10^{-2} Pa) at room temperature.

The inset of Fig. 2 shows the back-gate voltage (V_{bg}) dependence of the conductance (G) of an MLG device with thickness of 1.0 nm (~ 3 layers). The top gate was grounded. The minimum conductance at V_{bg} ~ 20 V corresponds to the charge neutrality of the film, and the conductance increases almost linearly with decreasing V_{bg} below 0 V. The main panel of Fig. 2 shows the close-up of the top-gate voltage (V_{tg}) dependence of the conductance with the back gate grounded and the V_{bg} dependence of the conductance with the top gate grounded. From this figure, we obtain dG/dV_{bg} = 3.62 x 10^{-6} (S/V) around V_{bg} = 0, and dG/dV_{tg} = 5.20 x 10^{-7} (S/V) around V_{tg} = 0 .

3. Model

One can estimate the mobility of the top surface (μ_t) and that of the bottom surface (μ_b) of MLG, based on the following model. In this model, we divide the layers in the MLG in three parts: the layers near the top (bottom) surface with thickness λ (layer A (C)) and the remaining central part (layer B), as shown in Fig. 3, and we make two assumptions: 1) the mobilities of layers A to C (μ_t, μ_0, and μ_b, respectively) are constant over layers, and 2) The distribution of carrier density in each layer in the direction perpendicular to the surfaces is constant. These assumptions mean that the effect of the charged impurities as well as the gate electric fields reach the distance λ from the surface, so that λ is of the order of the interlayer screening length of MLG, λ_s ~ 1.2 nm[6].

Under these assumptions, the slope of the conductance for the back gate is given by

$$\frac{dG}{dV_{bg}} = \frac{d\sigma_b}{dV_{bg}}\frac{w\lambda}{L} = \frac{dn_b}{dV_{bg}}\lambda e\mu_b\frac{w}{L} = C_{bg}\mu_b\frac{w}{L}. \quad (1)$$

Here $\sigma_b = n_b e \mu_b$ is the conductivity in layer C (n_b: carrier density of layer C), w is the width of the MLG, and L is the separation of the voltage leads. $C_{bg} = \varepsilon_r \varepsilon_0 / t_b$ is the back gate capacitance for unit area, where $\varepsilon_r = 3.9$ is the relative dielectric constant of SiO_2, ε_0 the dielectric constant of vacuum, and t_b is the thickness of SiO_2. In the same way, the slope of the conductance for the top gate around $V_{tg} = 0$ becomes

$$\frac{dG}{dV_{tg}} = C_{tg}\mu_t \frac{wL_t}{L^2}, \qquad (2)$$

where L_t is the length of the top gate along the current flow (see Fig. 3), and $C_{bg} = \varepsilon_0 / t_t$ is the top gate capacitance per unit area with t_t the height of the top gate.

For the sample of Fig. 2, $L_t = 1.0$ μm, $L = 4.2$ μm, $w = 1.27$ μm, $t_t = 0.21$ μm, $t_b = 0.30$ μm, giving $\mu_t = 2630$ cm^2/Vs, $\mu_b = 1290$ cm^2/Vs, and the ratio, $r = \mu_b / \mu_t = 0.49$. In fig. 4, we show the dependence of r on the MLG thickness t for six samples. The thickness of thin samples (1.0 and 1.3 nm) was estimated from the contrast of SEM images, and that of other samples from the atomic force microscopy. The ratio $r < 1$ for all samples indicates that the influence of the SiO_2 substrate on the mobility is stronger than that of adsorbates and contaminations on the top surface of the MLG. The larger r for the 1-nm MLG is due to the fact that the thickness t is close to λ_s.

4. Summary

We studied the mobilities of the top and bottom surfaces of MLG. The top mobility is larger than the bottom mobility for all samples, indicating that the SiO_2 substrate is the main cause of the low mobility in graphene.

References

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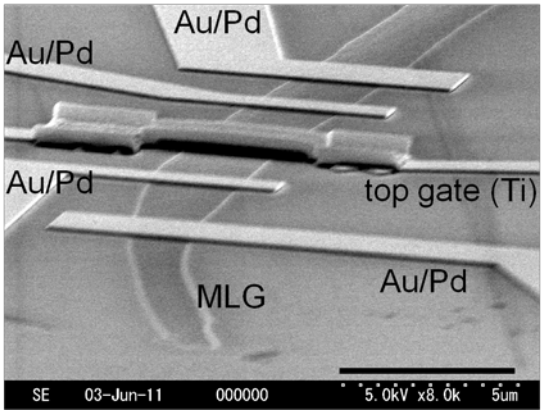

Fig. 1. SEM image of a dual-gated MLG.

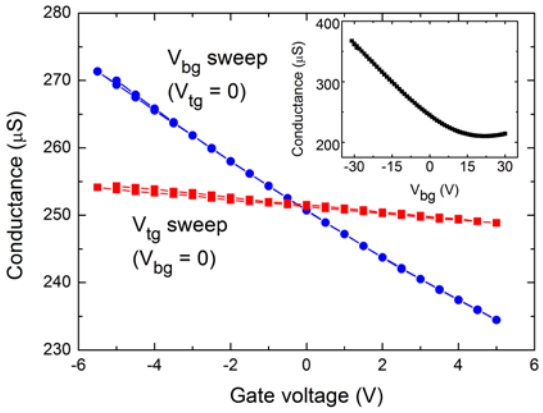

Fig. 2. Top and back gate dependences of the conductance. (Inset) Back gate dependence of the conductance for larger gate voltages.

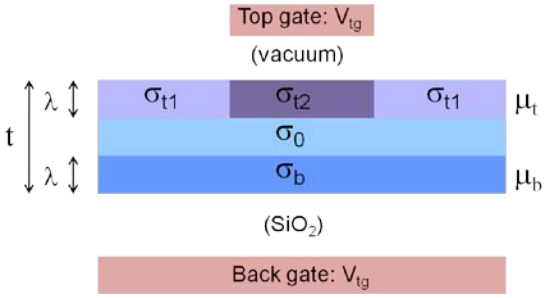

Fig. 3. Model for the calculation of μ_t and μ_b.

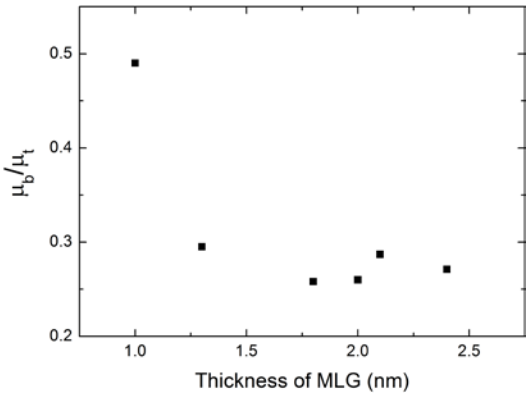

Fig. 4. Thickness dependence of the mobility ratio, μ_b / μ_t.