Tri-Gate Poly-Si TFTs Fabricated by CW Laser Lateral Crystallization for Improvement of Electron Transport Properties

Shuntaro Fujii, Yuya Kawasaki, Shin-Ichiro Kuroki, and Koji Kotani
Graduate School of Engineering, Tohoku University
6-6-05, Aza-Aoba, Aramaki, Aoba-ku, Sendai, 980-0857, Japan
Phone: +81-22-795-7122, Fax: +81-22-263-9396, E-mail: kuroki@eeci.tohoku.ac.jp

1. Introduction
High performance poly-Si TFTs with high mobility are required for system-on-glass applications. Laser crystallization is powerful technique for enlarging Si grains and enhancing mobility [1-5]. However, the mobility of laser-crystallized poly-Si TFTs varies due to the random crystalllographic orientation of the grains [1,2,4]. In this study, tri-gate structures, which are known as the structures that have high immunity against short channel effect [6], were introduced into poly-Si TFTs fabricated by CW laser lateral crystallization (CLC). The effects of tri-gate structures on effective electron mobility ($\mu_e$) in CLC poly-Si TFTs were investigated.

2. Specific Features of CLC Poly-Si Films
The specific features of crystallinity in CLC poly-Si films are summarized as follows: 1) as shown in Fig. 1 (EBSD mapping), the average grain size is $20\times2 \mu m^2$; 2) the crystal growth direction, which is the same as the CW laser scanning direction, tends to take $<110>$ direction although the surface orientation is random [7]; 3) biaxial tensile strain is induced by the difference of thermal expansion coefficients between Si and SiO$_2$ [7,8]. The specific features of $\mu_e$ in planar CLC poly-Si TFTs are summarized as follows: 1) phonon scattering is dominant [3-5]; 2) the biaxial tensile strain enhances $\mu_e$ [5]; 3) $\mu_e$ variation depends on the gate length (L) and gate width (W), and is uniquely determined by the number of grains (N) in the channel regions as shown in Fig. 2.

3. Concepts of Tri-Gate Structure
Figure 3 shows a concept of $\mu_e$ enhancement by the tri-gate structure. It is reported that narrow mesa structures give uniaxial strain [9]. When the channel direction is parallel to laser scanning direction, further $\mu_e$ enhancement is expected because uniaxial tensile strain along $<110>$ direction is useful for $\mu_e$ enhancement on various surface orientation [9,10]. Fig. 4 shows a concept of reduction of $\mu_e$ variation by the tri-gate structure. By using the tri-gate structure, the number of surfaces with different crystal orientation increased at most three times. Based on Fig. 2, 42% reduction of $\mu_e$ variation at maximum is expected.

4. Device Fabrication
Figure 5 shows the process flow. In CLC process, cap SiO$_2$ films were used to reduce the surface roughness [11]. The channel direction was parallel to the CW laser scanning direction. The wire structures were fabricated by electron beam lithography and dry etching. Gate SiO$_2$ film of 30 nm was formed by dry oxidation at 1100$^\circ$C to reduce the corner effect [12]. It was confirmed that the oxidation process on Si films did not change its crystallinity and grain sizes by EBSD measurements. It was also confirmed that the 0.3% tensile strain remained after the oxidation process by XRD measurements. Figure 6 shows the layout. Table I shows the designed device parameters. Number of wires was 23. Wire thickness, width and space were 150, 150, and 300 nm, respectively. These parameters were chosen so that the effective channel width ($W_{eq}$) of tri-gate TFTs becomes the same as that of planar TFTs because $\mu_e$ variation depends on the channel size as shown in Fig. 2. In addition, the occupied area of tri-gate TFTs was the same as that of planar TFTs. Figure 7 shows the cross-sectional TEM images of the fabricated tri-gate TFTs.

5. Results
Figures 8 and 9 show $I_D-V_{DS}$ and $I_D-V_{GS}$ characteristics of the tri-gate TFTs. Normal MOSFET operation with on/off ratio of $7\times10^8$ was achieved. 15 tri-gate TFTs and 21 planar TFTs were measured. Then, the average $\mu_e$ and the $\mu_e$ variations were characterized. Figure 10 shows the average $\mu_e$ dependence on the surface carrier density ($N_s$). At $N_s$ larger than $3\times10^{12}$ cm$^{-2}$, average $\mu_e$ was enhanced by using the tri-gate structures. 8% and 17% $\mu_e$ enhancements were achieved at $N_s$ of $5\times10^{12}$ and $1\times10^{13}$ cm$^{-2}$. Figure 11 shows $\mu_e$ variation dependence on $N_s$. By applying the tri-gate structures, 41% reduction of $\mu_e$ variation was achieved at $N_s$ of $5\times10^{12}$ cm$^{-2}$. These results showed that tri-gate structure is useful for both $\mu_e$ enhancement and reduction of $\mu_e$ variation in the high performance poly-Si TFTs.

6. Conclusions
Tri-gate CLC poly-Si TFTs with tensile-strained grains were successfully operated. Both 8% $\mu_e$ enhancement and 41% reduction of $\mu_e$ variation were achieved by applying the tri-gate structure. These results are useful for device size shrinkage of the high performance poly-Si TFT integrated circuits.

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References
Fig. 1 EBSD mapping of a CLC poly-Si film.

Fig. 2 $\mu_e$ variation dependence on (a) channel size and (b) $N$. The channel direction was parallel to the CW laser scanning direction. For each channel size, 15 – 40 planar CLC poly-Si TFTs whose fabricated process was shown in [5] were measured.

Fig. 3 Schematic image of the top-views. Effect of the tri-gate structures is the $\mu_e$ enhancement by introducing uniaxially tensile strain along <110>.

Fig. 4 Schematic image of the cross-sectional views. The tri-gate structures is effective for the reduction of $\mu_e$ variation since the number of surfaces with different crystal orientation is increased.

Fig. 5 Process flow of the tri-gate CLC poly-Si TFTs.

Table I

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<thead>
<tr>
<th>Designed device parameters.</th>
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<tr>
<td>Structure</td>
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<tr>
<td>$L$ [µm]</td>
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<tr>
<td>$W_{0x}$ [µm]</td>
</tr>
<tr>
<td>Two-dimensionally occupied width [µm]</td>
</tr>
<tr>
<td>Number of wires</td>
</tr>
<tr>
<td>Wire width [nm]</td>
</tr>
<tr>
<td>Wire space [nm]</td>
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<td>Thickness [nm]</td>
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Fig. 6 Layout of the tri-gate TFT.

Fig. 7 Cross-sectional TEM images of the tri-gate TFT.

Fig. 8 $I_D-V_{DS}$ characteristics of the tri-gate TFT at room temperature.

Fig. 9 $I_D-V_{GS}$ characteristics of the tri-gate TFT at room temperature.

Fig. 10 Average $\mu_e$ of planar and tri-gate TFTs at room temperature.

Fig. 11 $\mu_e$ variation of planar and tri-gate TFTs at room temperature.