Extended Abstracts of the 2011 International Conference on Solid State Devices and Materials, Nagoya, 2011, pp1260-1261

K-1-6

Room Temperature Single Charge Memory by Carbon Nanotube Transistor With SiN_x /Al_2O_3 Wrapped Double Gate Insulator Layers

Takafumi Kamimura [1, 2, 3], Yutaka Hayashi[2, 3], and Kazuhiko Matsumoto [1, 2, 3]
[1] Osaka University, [2]CREST-Japan Science & Technology Agency and [3] National Institutes of Advanced Industrial Science and Technology.
E-mail: kamimura@sanken.osaka-u.ac.jp

We have succeeded in observing the single charge memory effect at room temperature by fabricating the single walled carbon nanotube (SWNT) transistor with wrapped double gate insulator layers and with short gate electrode length of 10nm.

The fabrication process of the single charge memory is shown in Fig. 1(a). The device was fabricated as follows. The SWNT was grown by the chemical vapor deposition process on the SiO_2 substrate. The SWNT bridge was formed between source and drain electrodes by chemical etching of the SiO_2 under the SWNT. Then, the SWNT was wrapped around by double-layers of SiN_x of 27 nm over Al_2O_3 of 3 nm using atomic layer deposition process (FlexAL, Oxford inst.). The top gate electrode of 10 nm length is realized on the insulator as shown in Fig. 1(a) and (b).

Figure 2(a) and (b) show simulated electric field intensity by finite element method (Amaze, Advanced Science Laboratory, Inc.). Fig. 2(a) shows electric field intensity in y – z plane, which is corresponding to the plane shown in Fig. 1(b). The simulated electric field is strong just under the top gate electrode of 10 nm length. Therefore, the top gate affects locally around the SWNT and the insulator. Fig. 2(b) shows electric field intensity in x – z plane. The inset of Fig. 2(b) is the schematic of cross sectional view (x – z plane) of A – A' line in Fig. 1(b). The shape of top gate electrode is semi-wrapped structure around concentric layers of the SWNT, the Al_2O_3 and the SiNx as shown in inset of Fig. 2(b). Though the top gate electrode covered only half of the concentric insulator layers, the electric field intensity is fully strong because of electric field concentration by the device structure.

Figure 3 shows drain current characteristic as a function of the applied top gate voltage at room temperature. The source and drain voltage are set at -25 mV and 25 mV, respectively. The drain current increases and the characteristic shifts discretely about 0.22 V with increasing applied top gate voltage. This discrete shift of the drain current is attributed to the threshold voltage shift caused by one charge stored in trap site between the Al_2O_3 layer and the SiNx layer. The interface state of 1×10^{12} cm^{-2} densities estimated from the C - V measurement is at between the Al_2O_3 layer and the SiNx layer. The area just under the top gate electrode is 91.4 nm^2 from πrL, where r is thickness of the Al_2O_3 layer, L is length of the top gate electrode. Therefore, about one interface state exists at the area just under the top gate electrode. Moreover, the threshold voltage shift caused by one charge stored in the interface state is given by $\Delta V_{th} \sim e/(C_{gi} + C_{gSWNT})$, where C_{gi} and C_{gSWNT} is mutual capacitances of the top gate electrode and the interface state and of the top gate electrode and the SWNT as shown in the inset of Fig. 3. C_{gi} and C_{gSWNT} are estimated to be 734 zF and 20.7 zF, from the simulation of the finite element method, where 1 nm diameter conductor sphere at 3 nm above the SWNT was assumed in the simulation as the single interface state. The threshold voltage shift was estimated to be 0.201 V. This is in good agreement with the threshold voltage shift of the drain current characteristic as shown in the Fig. 3.

Figure 4 shows the hysteresis width as a function of absolute value of the applied round-trip top gate voltage. Inset of Fig. 4 shows the drain current characteristic as a function of the applied round-trip top gate voltage, which shows hysteresis characteristic. The hysteresis width increases discretely with applied round-trip top gate voltage. The unit of the discrete change of the hysteresis width is about 0.22 V, which is same value of the threshold voltage shift as shown in Fig. 3. The difference of the trap and release voltage of the stored charges in the interface state causes the hysteresis characteristic and the hysteresis width determined by the number of the stored charges.

Figure 5(a) shows the schematic (top) and the measurement (bottom) of the erase and write/read states cycles, where the write state is top gate voltage of 1 V and applied time was parameter ranged from 0.1 sec to 1000 sec, the read state is top gate voltage of 0 V for 10 sec and the erase state is top gate voltage of -4 V for 60 sec. Fig. 5(b) shows the drain current value at the read state as a function of the write time. The drain current increases discretely with increase of the write time, and almost saturates in the longer and shorter write time. The charging phenomenon is attributed to the tunneling effect through Al_2O_3 layer. When the write time is too short, the charge can hardly tunnel enough and drain current change is small. When the write time is long enough, several charges up to 5 charges can tunnel to the interface state in sequence, and finally the potential energy of the trap site come near to that of the SWNT, and the tunneling is blocked by the Coulomb blockade. Then, the drain current reached high level and saturated. The schematic tunneling process is shown in Fig. 5 (c). The transition region of the drain current in Fig. 5(b) attributed to the stochastic discrete charge tunneling. The tunneling processes comply with the Poisson process under the assumption of that each tunneling processes are independent. The tunneling probability per unit time as a function of the number of the tunneling charges from the SWNT to the interface state is estimated from Fig. 5(b) and the Poisson distribution as shown in Fig. 5(c).

After the constant top gate voltage is applied, the drain current stays constant value, even though the top gate voltage is turned back to 0 V as shown in Fig. 4. This is the memory effect by the single charge trap. At least three discrete levels in the drain current show the memory effect. In this measurement, each voltage is applied for 60 min and the peak of the drain current value distribution is plotted as shown in Fig. 4.

In conclusion, we have fabricated the SWNT transistor with the wrapped double gate insulators and with the ultra-short gate electrode of 10 nm. The device shows the multi-level memory effect owing to the single charge trapping effects at room temperature.

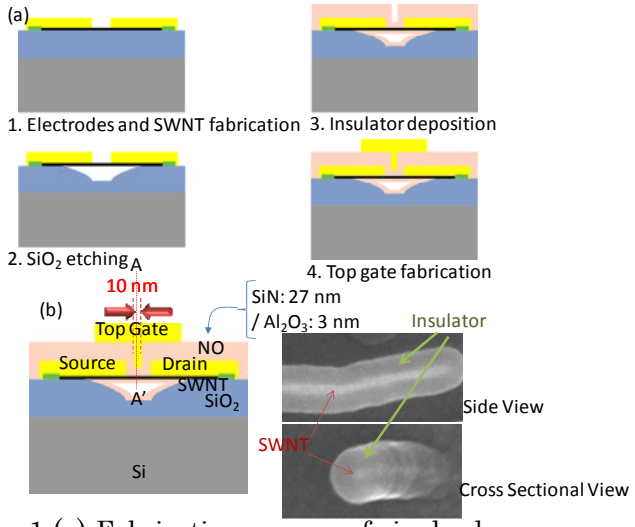

Fig. 1 (a) Fabrication process of single charge memory. (b) Schematic of single charge memory and insulator around SWNT by scanning electron microscope images.

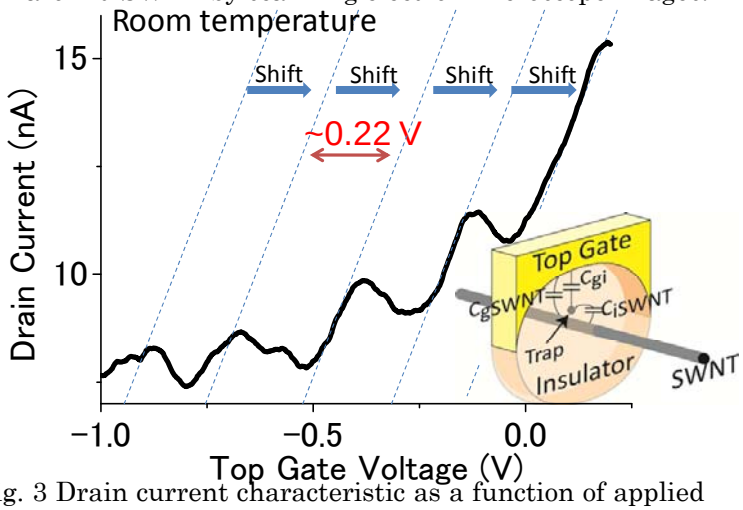

Fig. 3 Drain current characteristic as a function of applied top gate voltage. Inset: mutual capacitances of gate – interface state, gate – SWNT and interface state - SWNT.

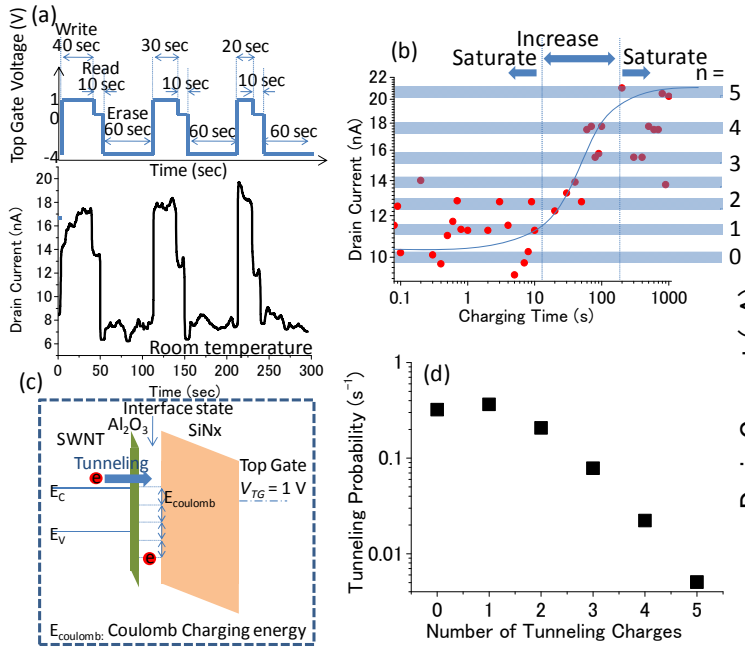

Fig. 5(a) schematic (top) and the measurement (bottom) of the erase and write/read states cycles. (b) The drain current value at the read state as a function of the write time. (c) Schematic of tunneling process. (d) Tunneling probability as a function of number of tunneling charges estimated from Poisson distribution and Fig. 6(b).

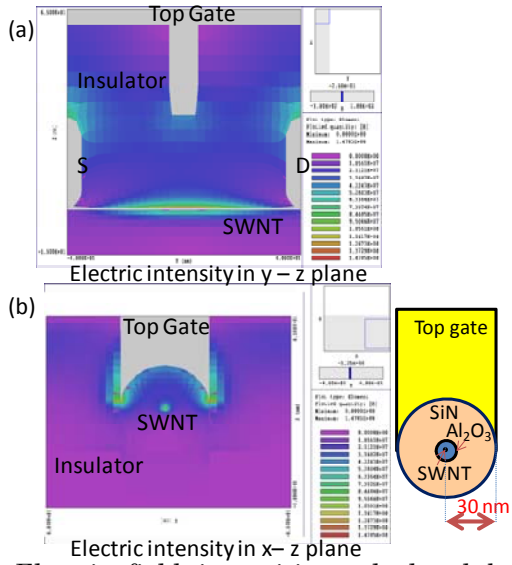

Fig. 2 Electric field intensities calculated by finite element method. (a) in y – z plane and (b) in x– z plane. Inset: Schematic of cross sectional view (x – z plane) of A – A' line in Fig. 1(b).

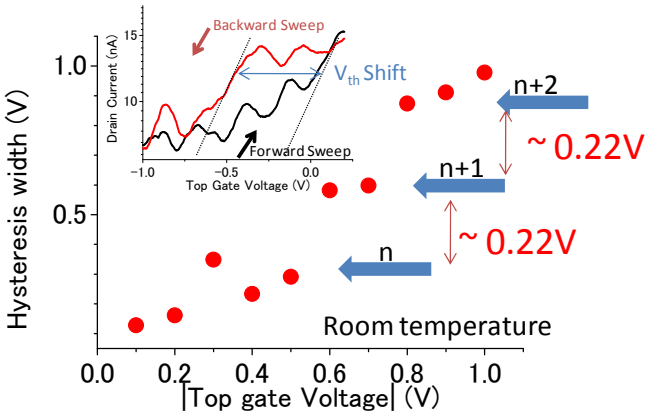

Fig. 4 Hysteresis width as a function of absolute value of round-trip top gate voltage. Inset: Drain current characteristic as a function of the applied round-trip top gate voltage.

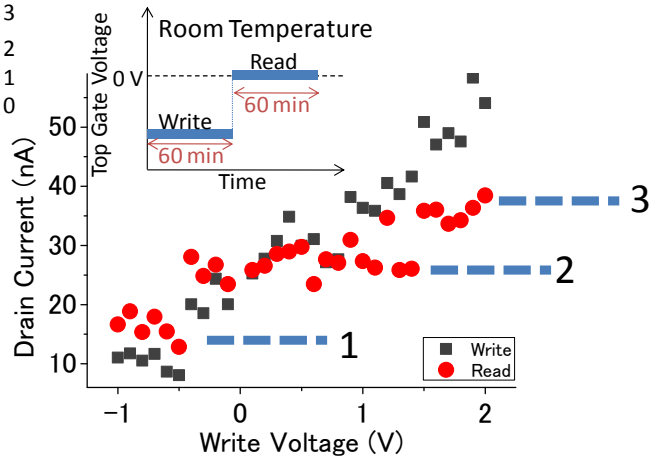

Fig. 6 Memory effect by the single charge trap. After the constant top gate voltage (write state: glary square) is applied, the drain current stays constant value, even though the top gate voltage is turned back to 0 V (read state: red circle).