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High-performance Carbon Nanotube Thin-film Transistors with >600 $cm^2V^{-1}s^{-1}$ Mobility and >10^7 On/off Ratio

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1. Introduction

Carbon nanotubes (CNTs) with the extraordinary material properties are capable of being an active layer of thin-film transistors (TFTs) to fabricate high-performance, flexible, and transparent electronic devices with relatively simple techniques. Previously, we have presented a simple technique of the gas-phase filtration and transfer process to fabricate the CNT TFTs, demonstrated logic integrated circuits (ICs) on a flexible and transparent substrate, including a 21-stage ring oscillator and master-slave delay flip flops [1]. Here, we report high-performance CNT TFTs with quite high-mobility and on/off ratio simultaneously. We also discuss the evaluation methods for the carrier mobility and the key factors for achieving the high on/off ratio.

2. Device Fabrication

The CNT TFTs were fabricated by a gas-phase filtration and transfer process [1]. The single-walled CNTs were continuously grown using floating-catalyst (aerosol) chemical vapor deposition (FC-CVD) [2] and collected on a membrane filter at room temperature and atmospheric pressure. The CNT thin film was transferred onto the SiO_2/Si substrate, on which the TFT electrodes had been prepared, by dissolving the filter in acetone. Subsequently, the CNTs outside the channel area were removed by oxygen plasma etching so that each device was electrically separated.

3. Carrier Mobility Evaluation

Figure 1 shows I_D-V_{GS} and I_D-V_{DS} characteristics of a typical CNT TFT. The CNT TFT shows p-type characteristics with the on/off ratio of 2×10^7. The carrier mobility μ can be evaluated from the linear region of direct current (DC) characteristics by the standard formula,

$$\mu = \frac{L_{ch}}{W_{ch}} \frac{1}{C} \frac{1}{V_{DS}} \frac{dI_D}{dV_{GS}} \quad (1)$$

where L_{ch} and W_{ch} are the channel length and width, V_{DS} and V_{GS} the bias voltage and gate voltage, I_D the current, and C the gate capacitance per area, respectively.

There are two models to estimate C: the parallel plate model and a more rigorous model, as shown in Fig. 2. In the former model, the CNT thin film is assumed to be a homogeneous sheet, and the gate capacitance is expressed as,

$$C_P = \varepsilon\varepsilon_0 / t_{ox} \quad (2)$$

where t_{ox} and $\varepsilon\varepsilon_0$ are the thickness and dielectric constant of the gate insulator respectively. By the parallel plate model, the mobility of the present TFT is evaluated to be 35 $cm^2V^{-1}s^{-1}$. In the case of CNT TFTs used in our study, however, the effective coverage of CNT film, $\rho_{CNT}L_{CNT}^2$ [3], is quite low, i.e. ~10 (here, ρ_{CNT} and L_{CNT} are the density and length of CNTs). This corresponds to the coverage of ~1.5% for the CNT diameter of ~1.5 nm. Then, the parallel plate model overestimates the gate capacitance.

A more rigorous model which takes into account the realistic electrostatic coupling between sparse CNTs and the gate electrode [4] should be used for present devices. In this model, the gate capacitance is given by

$$C_R = \left\{ C_Q^{-1} + \frac{1}{2\pi\varepsilon\varepsilon_0} \ln\left[\frac{\Lambda_0}{R} \frac{\sinh(2\pi t_{ox}/\Lambda_0)}{\pi} \right] \right\}^{-1} \Lambda_0^{-1} \quad (3)$$

where C_Q is the quantum capacitance of CNTs, Λ_0 is the linear density of CNTs, and R is the radius of CNTs. For the present CNT TFTs, Λ_0 = 0.54 tubes/μm, R = 0.75 nm, and then, the gate capacitance becomes lower than those given by the parallel plate model as C_R/C_P = 1/18. The mobility is evaluated to be 634 $cm^2V^{-1}s^{-1}$ based on the rigorous model.

4. On/off Ratio

The on/off ratios of present CNT TFTs were typically 10^6~10^8, a few orders of magnitude higher than conventional solution-based CNT TFTs [5], even though as-grown CNTs (~30% metallic CNTs) were used. The high on/off ratio was realized by the CNT density precisely controlled by adjusting collection time in the FC-CVD technique. A-few-second collection time makes the metallic CNT density lower than the percolation threshold.

In addition, the high on/off ratio may be achieved with clean CNTs, without contaminations usually introduced in the solution processes. To confirm this, a TFT was contaminated by soaking into 1% solution of sodium dodecyl sulfate (SDS) which is a type of surfactants commonly used to disperse CNTs in water. After soaking for 12 h, the on/off ratio decreased from 10^7 to <10^3. Moreover, the on-current and transconductance decreased, and the threshold voltage shifted. SDS causes charge traps around the

CNTs, so that the electric force lines from the gate terminate at the traps, thus the modulation effect of V_{GS} is restricted. Therefore, the clean CNTs are important to realize high on/off ratio of TFTs.

Also, we investigated the on/off ratio degradation phenomenon at a high V_{DS} [5]. The on/off ratio was degraded from 10^8 to $>10^5$ by electron minority current with increasing V_{DS} (Fig. 3(a)). The degradations can be relatively suppressed by using CNTs with smaller diameter (1.1 nm). The on/off ratio of 10^7 was achieved at an operation voltage of ICs (V_{DS} = −5 V), as shown in Fig. 3(b).

The energy bandgap (E_g) of a semiconducting CNT is inversely proportional to the diameter. E_g are ~0.49 and ~0.71 eV for $2R$ = 1.6 and 1.1 nm, respectively. As shown in the insets of Fig. 3(a,b), electron injection through the barrier between the conduction band and Fermi level of the metal is suppressed for the larger E_g, and thus the on/off ratio degradation is suppressed. The statistical study regarding the on/off ratio distributions of 60 TFTs were carried out to verify the above results.

5. Conclusions

We discussed the detailed characteristics including the carrier mobility and on/off ratio of the CNT TFTs fabricated by the simple filtration and transfer process. The mobility evaluation based on the rigorous model is appropriate for the present devices with low coverage of CNTs, rather than that based on the parallel plate model. The mobility was as high as 634 cm^2/Vs. The high on/off ratios of 10^6~10^8 were realized. The key factors for the high on/off ratio are the precise control of the CNT density and the use of clean CNTs. The smaller-diameter CNTs are preferable to suppress the on/off ratio degradation at higher operation voltages.

Acknowledgements

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References

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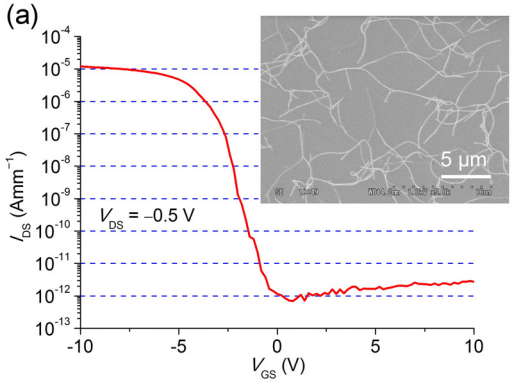
Figures



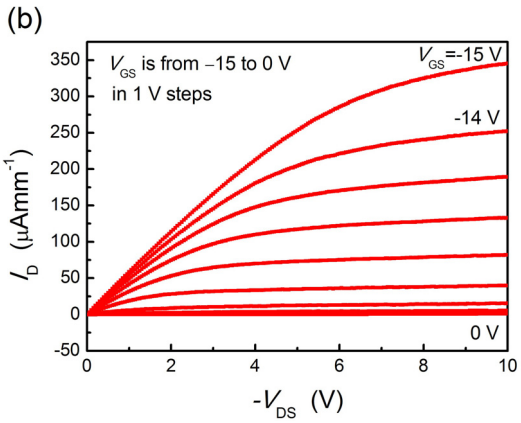


Fig. 1 (a) Transfer and (b) output characteristics of a CNT TFT. The inset of (a) is an SEM image of CNT film.

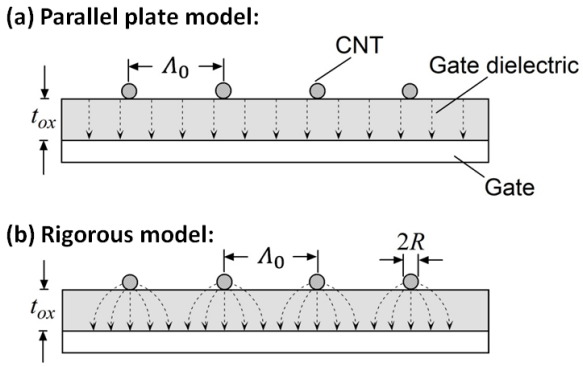


Fig. 2 Schematics of electric force lines in (a) parallel plate model and (b) rigorous model.

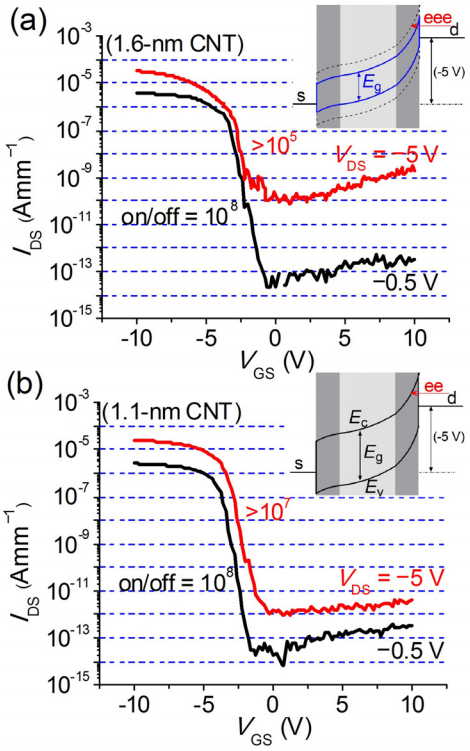


Fig. 3 Typical I_D-V_{GS} characteristics at V_{DS} of −0.5 and −5 V. (a) CNT diameter of 1.6-nm, (b) 1.1-nm. The insets show schematic band diagrams of electron tunneling.