Extended Abstracts of the 2011 International Conference on Solid State Devices and Materials, Nagoya, 2011, pp1286-1287

Graphene Growth on Sidewall of Catalyst by CVD and Its Application to Graphene Transistors

Hyosub An[1], Wan-Gyu Lee[2] and Jongwan Jung[1*]

[1] Institute of Nano and Advanced Materials Engineering, Graphene Research Institute, Sejong Univ.
98, Gunja-dong, Gwangjin-Gu, Seoul 143-747, South Korea
Phone: +82-2-3408-3688 E-mail: *jwjung@sejong.ac.kr
[2] National Nano Fab Center

1. Introduction

Graphene, a flat mono atomic layer of carbon atoms has a high electron mobility that could lead to exceptionally fast transistors, or ultra thin and/or transparent electrodes. [1,2] There have been several reports regarding graphene synthesis.[3,4] Among them, chemical vapor deposition (CVD) on metal catalyst is very promising, owing to its high film quality and its easy scale-up. However, to implement CVD-grown graphene ribbons, transfer process is necessary due to the metal catalyst beneath the synthesized graphene layer. A general wet transfer method includes detaching of graphene film from the metal catalyst, and transferring it onto a desired substrate. Even though roll-to-roll transfer techniques have been reported recently,[5] an inexpensive and high-throughput transfer method without generating folding and defects is still highly challenging. In this paper, a novel method for implementing graphene ribbons out of CVD-grown graphene is proposed, which does not require the transfer processes. In this method, the metal catalyst is pre-patterned before CVD synthesis, and the graphene synthesized on the sidewall of the catalyst is used for graphene ribbons. Since resultant graphene ribbons are fin-shaped, real dual gate graphene transistors might be easily implemented.

2. Fabrication

The schematic overall process flow for the proposed graphene ribbon is shown in Fig.1. The process started with depositing a 300 nm- thick SiO_2 on a Si substrate. Then a 300 nm-nickel (Ni) and a 300 nm- SiO_2 were sequentially deposited by sputtering and CVD, respectively. The Ni film acts as a catalyst for graphene growth, and the top 300 nm-SiO_2 as a blocking layer to protect the top surface of Ni catalyst from graphene synthesis. The oxide/Ni stack was patterned by lithography and etched Fig.1(a),(b). Through these steps, only the sidewalls of the Ni catalyst were exposed, upon which graphene would grown by CVD. Few-layer graphene was grown by rapid thermal CVD system with a 2 inch-horizontal quartz tube Fig.1(c). After graphene synthesis, PMMA was coated and etched-back carefully to expose only the cap oxide upon Ni Fig.1(d). Then, the cap oxide and the PMMA was removed sequentially by dry etcher and acetone, respectively Fig.1(e). After that, SOG(spin on glass) film, acting as a supporting film of the resultant graphene ribbon was coated and etched back Fig.1(f). Graphene channel was patterned by lithography. Then, the exposed Ni was removed using $FeCl_3$-based Ni etchant Fig.1(g), resulting in two parallel graphene ribbons. In order to see top gate modulation characteristics of the resultant graphene ribbons, SOG as a gate dielectric was coated and Al as a top gate metal was deposited Fig(h).

When compared to the conventional CVD process for graphene ribbon transistors, this process does not require the graphene transfer process since the sidewall- graphene is used. Besides, since ribbons are fin-shaped vertical, real dual gate graphene transistors might be easily implemented. In order to identify extremely thin graphene layers on the sidewall of the metal, transmission electron microscope (TEM), and Raman spectroscopy was used. I-V measurements of ribbons and ribbon transistors were performed by semiconductor analyzer (Agilent B1500A).

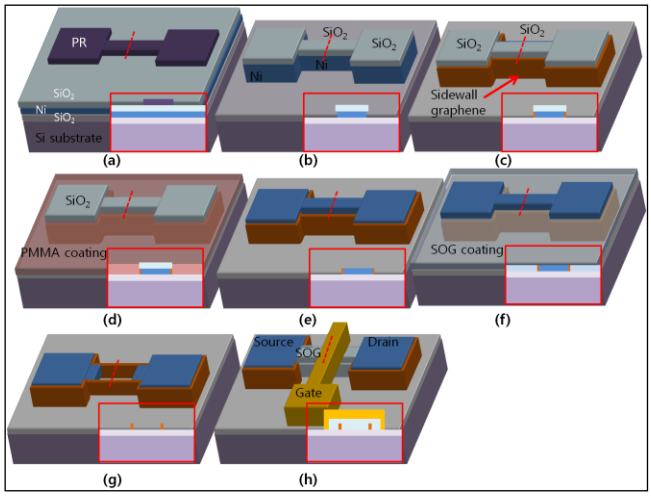

Fig. 1 Schematic for synthesizing graphene ribbons on the sidewall of Ni. (a)-(g) are indicating overall process explained above and (h) is representing an additional process after formation of top gate. Cross-section of each three dimensional image which is described by dotted red line is illustrated in each red frame inset.

3. Results and Analysis

The resultant sample images during each process step are shown in Fig.2. As shown in Fig.2, the Ni catalyst can be spotted between the cap and the bottom SiO_2. In order to confirm if the Ni was completely etched out, I-V curves of ribbons were measured before etching Ni and after as

shown in Fig.3(a),(b). Using Raman analysis , we also have identified the presence of graphene on the sidewall as shown in Fig.3(c). Because of lower growth temperature (600°C), this sample shows high D-peak. We also confirmed that negligible currents flow for samples for which CVD was skipped after Ni etching Fig.3(b).

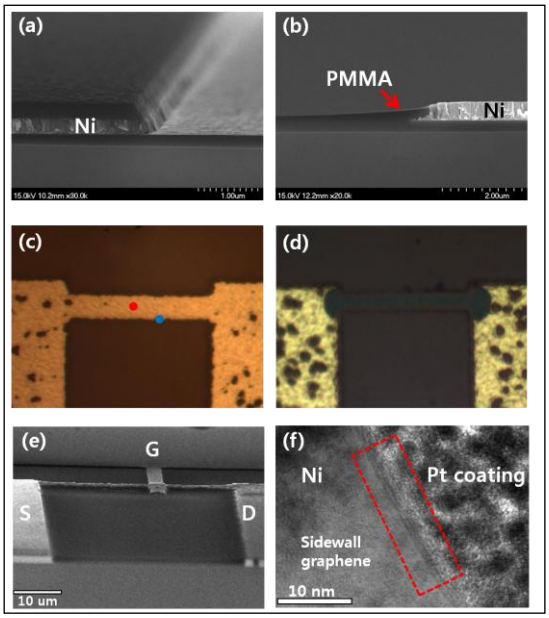

Fig. 2 (a)-(e) SEM and optical microscope images of the samples during process steps. (a) After patterning SiO_2/Ni layer (corresponding to Fig.1(b)), (b) after PMMA coating and etch-back to expose the cap oxide upon Ni (corresponding to Fig.1(d). (c),(d) Before and after etching Ni catalyst. (e) The fabricated top-gated graphene transistor using sidewall graphene ribbon. (f) TEM image of the synthesized few-layer graphene on the sidewall of Ni.

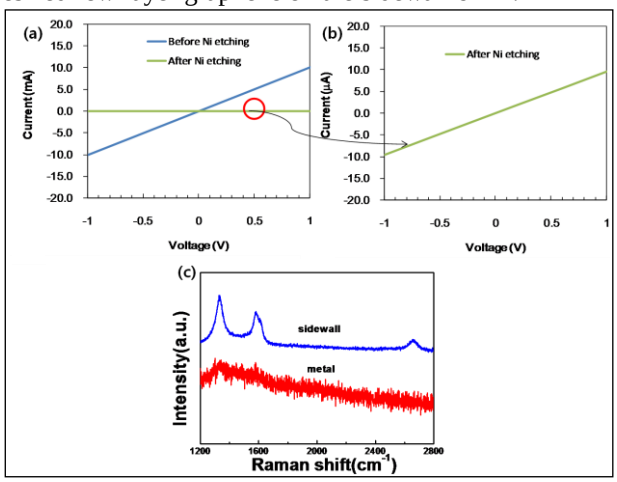

Fig.3 I-V curve of a fabricated ribbon before etching Ni (blue) and after (green). (b) Scaled I-V curve for green line of (a). (c) Raman analysises of the metal and sidewall at the regions indicated in Fig.2(c) by red and blue dots respectively correspond to red and blue lines in Fig.3(c).

Figure 4(b), and (c) are typical output and transfer characterisics operating in back-gate configuration. It can be shown that drain currents are modulated with the back gate voltages. The dirac voltage was measured to be shifted to +10V, indicating p-type graphene. For top-gate transistors, they did not show gate-modulated characteristics due to extremely high gate leakage current. It is expected that greatly enhanced output characteristics would be achieved if the ribbons were modulated by top gate oxide. Further experiments for reliable ribbons with top gate are underway.

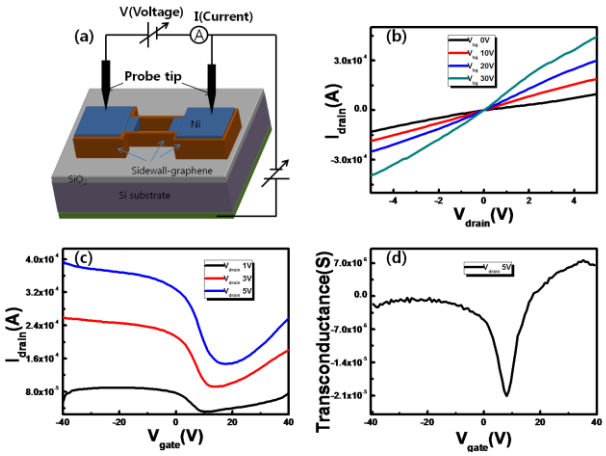

Fig.4 Back-gate modulation characteristics of a fabricated sidewall- graphene ribbon

4. Conclusions

A novel method for implementing graphene ribbons using sidewall growth on the metal catalyst by CVD has been proposed, which does not require the transfer processes. In this technique, the Ni catalyst is pre-patterned before CVD, and sidewall-graphenes synthesized on the Ni is used for graphene ribbons. Since the resultant ribbons are fin-shaped, real dual gate graphene transistors might be readily implemented. The fabricated graphene ribbon transistors showed gate–modulated output characteristics.

Further experiments for more vertical and reliable ribbons are underway.

Acknowledgements

This work was supported by the National Research Foundation of Korea (NRF) grant funded by the Korea government (MEST) (No. KRF-2008-313-D00383) and (No. 2010-0000141). This work was also supported by Priority Research Centers Program through the National Research Foundation of Korea (NRF) funded by the Ministry of Education, Science and Technology (2010-0020207).

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