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Electron tunneling in bilayer graphene *p-n* junction controlled by gate electric field

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1. Introduction

Control of the energy-band profile in semiconductors is one of the basic features of semiconductor electronics [1]. Unlike conventional *p-n* control in normal semiconductors, the ambipolar nature of graphene enables a control of the carrier polarity in an atomic film by modulation of the gate electric field without impurity doping [2]. A *p-n* junction can be formed by spatially modulating the electric field. One of the important advantages of such a *p-n* junction is that both the carrier density in each homogeneous (*p*-type or *n*-type) region and the potential profile are gate-tunable. This feature allows for flexibility in designing the potential profile in the graphene *p-n* junction because the profile can be designed in the geometry of the gate electrodes.

2. Experimental

Spatial gate modulation is introduced by changing the thickness of the top gate insulator by step (Fig. 1). A Si substrate supporting graphene is used as a back gate electrode. An electric field between the top and back gate induces band gap in graphene, if the graphene channel is bilayer [3,4]. In this case, an insulating region appears at *p-n* interface. A graphene sample with multiple electrodes was patterned by oxygen plasma etching for four terminal measurements. The top gate was composed of two regions with different gate dielectric thicknesses. Half of the area of the graphene channel was covered by a 5-nm-thick layer of SiO_2 (Fig. 2). Then, the entire area of the graphene between the voltage terminals was covered by a 30-nm-thick Al film (Fig. 3). The sample was exposed to air for several hours for partial oxidization of the Al film. An oxidized (AlO_x) layer formed not only on the surface but also at the inter-

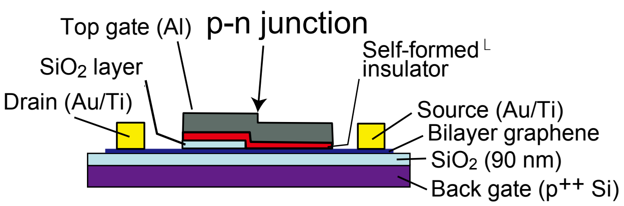

Fig. 1. Schematic draw of a graphene *p-n* junction controlled by stepwise top gate. The bottom surface of Al (top gate) electrode is naturally oxidized and insulates the top gate from the graphene [4]. The stepwise top gate structure is made by an additional SiO2 layer which covers the graphene channel partly.

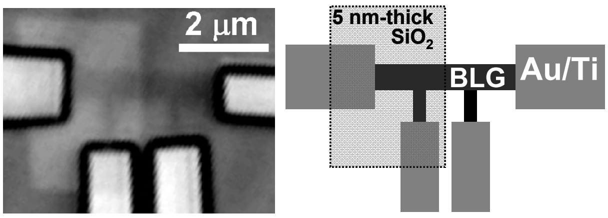

Fig. 2. Laser microscope image (left) and schematic draw of bilayer graphene covered partially by 5 nm-thick SiO_2. The graphene is patterned by oxygen plasma and contacted by Au/Ti electrodes for four-terminal measurement, followed by the SiO_2 deposition.

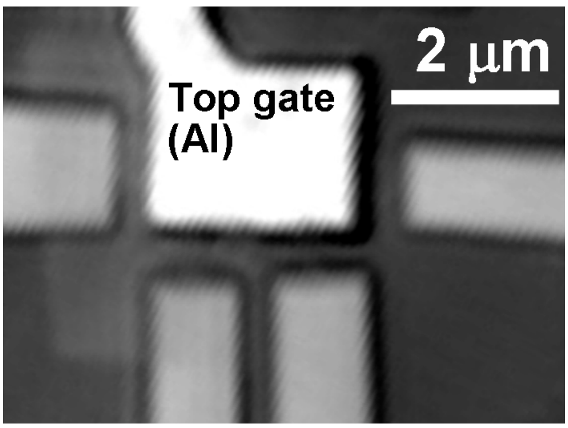

Fig.3. Laser microscope image of a bilayer graphene *p-n* junction. An Al top gate is deposited on the structure in the Fig. 2.

faces of Al/graphene [5] and Al/SiO_2 [6].

The differential resistance dV_{ds}/dI as a function of the source drain voltage V_{ds} was focused on. We found a peak in the dV_{ds}/dI curve for a forward bias (Fig. 4). This peak was not observed in monolayer or bilayer in which the band gap is not fully opened.

3. Discussions

We attribute this peak to the tunneling current between *p* and *n* regions similar to what is observed in an 3D Esaki diode [7]. The tunneling current at *p-n* tunnel current has a peak, i.e negative differential resistance (NDR), at forward bias. In our sample, leakage current via localized states in the band gap is comparable to the tunneling current, changing the NDR to the differential resistance peak.

4. Conclusions

We observed clear tunneling signals in semiconducting BLG *p-n* junctions. This provides an experimental evidence for the existence of insulating barrier in graphene at the *p-n* interface. We also identified localized states as the source of the diffusion current within the band gap, which highlights the importance to exclude the impurities and disorder in graphene to improve performance.

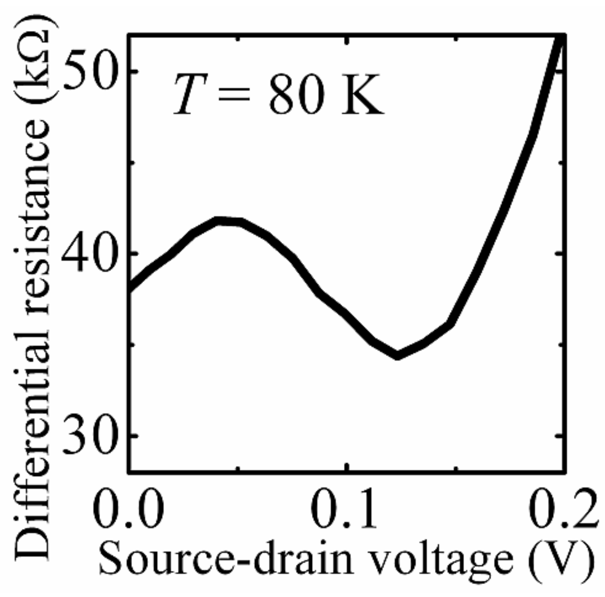

Fig.4. Differential resistance as a function of the source-drain voltage.

Acknowledgements

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