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High-Frequency Characterization of Vertical InAs Nanowire Wrap-Gate FETs on Si(111) Substrates

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1. Introduction

This paper addresses a III-V MOS technology based on nanowires. Here, the high mobility and injection velocity of InAs and the improved electrostatic control of wrap-gates are combined in a vertical InAs nanowire FET.

Previously, we have reported excellent DC characteristics for vertical InAs nanowire FETs on InAs substrates with g_m = 600 mS/mm and *SS* = 80 mV/dec[1], and, good high frequency characteristics on semi-insulating InP substrates with f_t > 7 GHz and f_{max} > 20 GHz[2]. Now, the technology is transferred to Si substrates utilizing a thin epitaxial InAs buffer layer. Electrical characterization of the fabricated devices show f_t = 9.3 GHz and f_{max} = 14.3 GHz. This is, to the authors' knowledge, the highest f_t reported for any vertical nanowire transistor. Further details are published elsewhere[3].

2. Device Fabrication

Growth of Vertical InAs Nanowires on Si

Nanowires are integrated on Si substrates by first growing a 260-nm-thick epitaxial InAs layer on a highly resistive Si(111) substrates. The InAs layer is grown by MOVPE and doped with Sn. Several nucleation layers, annealed at a high temperature, are used for achieving a smooth surface[4]. Nanowire seed particles are deposited on the InAs layer by EBL, Au deposition and lift-off. The seed particles are placed to form arrays of 190 nanowires for each transistor. The nanowires are grown by MOVPE with Sn-doping to a diameter between 25 nm and 40 nm, and a length of about 1 µm, see Fig. 1a.

Fabrication of Vertical Nanowire MOSFETs

The nanowire arrays function as multiple active channels in the transistor with source at the bottom, gate in the middle, and, drain at the top as illustrated by Fig. 2. To isolate the gate from the channel, a 6-nm-thick HfO_2 gate dielectric is deposited on the nanowires by ALD. Epitaxial source contacts are formed by UV-lithography and wet etching in the planar InAs layer to provide device isolation. The transistors use sputtered W wrap-gates with $L_g \approx$ 250 nm, defined by a RIE etch back process, and Ti/W/Au drain contacts and probing pads. The terminals are separated vertically by organic spacers, and, the metal layers are patterned by UV-lithography in a standard 50 Ω wave-guide layout as shown in Fig. 1b.

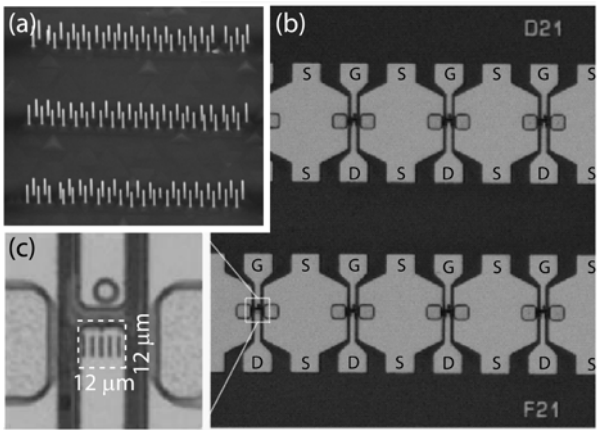

Fig. 1 (a) SEM-image of a nanowire array covered with HfO_2 at 30° tilt. The nanowire diameter is about 40 nm. (b) Micrograph of total 7 transistors, showing the 50 Ω wave-guide layout. (c) The 12 µm×12 µm box define the transistor cell for which the high frequency characteristics are deduced.

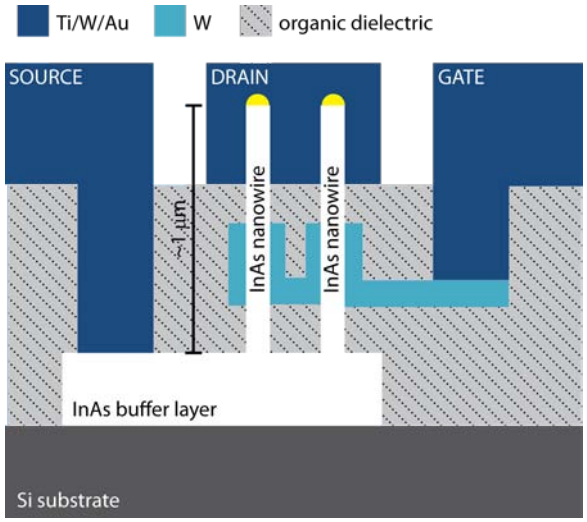

Fig. 2 Schematic cross-sectional illustration of the vertical InAs nanowire FET.

3. Electrical Measurements

Output characteristics measured by on-chip probing is shown in Fig. 3. The obtained peak transconductance is about g_m = 80 mS/mm and the on-current is I_{on} = 150 mA/mm. By introducing an annealing step after high-*k*

deposition, in forming gas at 300°C, the transconductance and on-current was increased to g_m = 155 mS/mm, and, I_{on} = 550 mA/mm, respectively, whereas, the on-off ratio was decreased. Statistics made on the annealed chip, which had a yield of 100% for the 190-nanowire transistors, showed only a slight decrease in normalized on-current and a strong increase in normalized transconductance as the nanowire diameter was scaled from 40 nm to 25 nm.

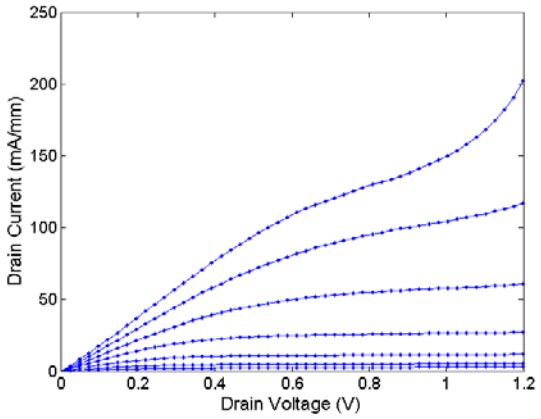

Fig. 3 The output characteristics for V_g varied between -1.5 V and 1.5 V in steps of 0.5 V.

Scattering parameters are measured from 60 MHz to 20 GHz using off-chip LRRM calibration and on-chip de-embedding. The de-embedded 12 µm ×12 µm transistor cell is shown in Fig. 1c. Unilateral power gain and, U, and current gain, h_{21}, for an annealed transistor is shown in Fig. 4. The extrinsic unity current-gain cut-off frequency is, f_t = 9.3 GHz and the maximum oscillation frequency, f_{max} = 14.3 GHz. This is to the authors' knowledge the highest f_t reported for any vertical nanowire transistor, although, still mainly limited to the large parasitic capacitances.

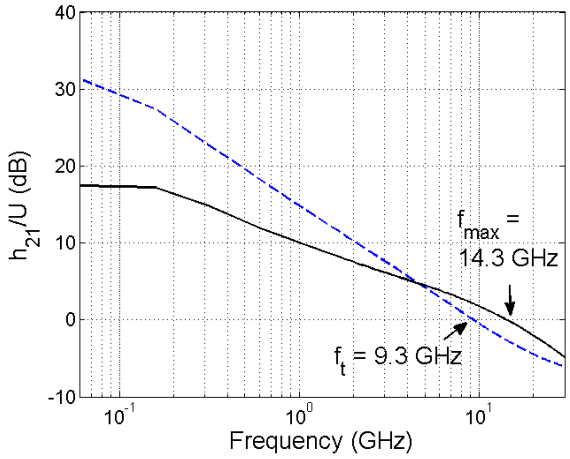

Fig. 4 Unilateral power gain, U, (solid curve) and current gain, h_{21}, (dashed curve) for a 12 µm×12 µm transistor cell show f_{max} = 14. 3 GHz and f_t = 9.3 GHz.

A small signal equivalent model is deduced from the measured data, consisting of a standard FET model and two frequency dependent current sources that account for impact ionization and band-to-band tunneling, following the approach in [5]. The model shows fairly good fit with the measured data, see Fig. 5.

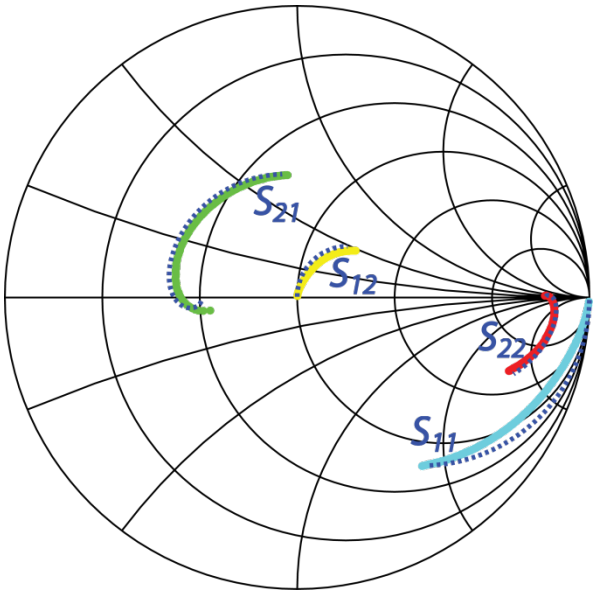

Fig. 5 Smith chart showing both measured (solid lines) and modeled (dashed lines) scattering parameters. The curls for low frequencies seen for S_{21} and S_{22} are modeled as impact ionization and band-to-band tunneling.

4. Summary

Vertical InAs nanowire FETs are successfully integrated on Si substrates by using a thin epitaxial InAs layer. Electrical characterization shows good DC performance in terms of transconductance, g_m = 155 mS/mm and on-current I_{on} = 550 mA/mm, and, good RF characteristics with f_t = 9.3 GHz and f_{max} = 14.3 GHz.

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