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A Novel FEM-LDMOS of Improved Off-state Breakdown Voltage Without Additional Mask

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1. Introduction

The power semiconductor industry has achieved rapid progress in the reduction of specific on-resistance ($R_{on,sp}$) and improvement of breakdown voltage in power MOSFETs, particularly in the low voltage range such as 30 V rating for display driver or DC–DC converter applications [1]. Recently, LDMOS (Lateral Double-diffused MOS) employing double RESURF (REduced SURface Field) technology using low thickness of EPI or N-Well has allowed the construction of high voltage devices with low on-state resistance [2]. Although there were many studies to improve characteristics of lateral devices, it still remains additional mask design and complex processes which both need more cost. We proposed the Focus-Energy-Matrix (FEM) methodology to increase off-state breakdown voltage and attain low on-resistance with mask free.

2. Device Fabrication

The FEM-LDMOS transistor fabrication process of defining p-buried layer is based on a 0.18-um high voltage (HV) CMOS technology developed by Vanguard International Semiconductor Corporation without any additional masks. The HV FEM-LDMOS with different PR length and standard devices without p-buried layer are both available in this technology.

Fabrication processes are shown in Fig.1. The starting wafer is a (100) oriented p-type wafer with doping concentration of 1×10^{15} cm^{-3}. The fabrication process begins with active region defined and is followed by shallow trench isolation formation (STI). Subsequently, HV p-well ion implantations are performed. The NDD-drift ion implantation is carried out after the p-well drive-in, because RESURF conditions [2], [3] require careful control of dose and junction depth. Gate lithography and etch, gate oxidation, polysilicon deposition, polysilicon gate etch, and doping annealing are then carried out to form the gate electrode. Then spacer side wall and source/drain anneling are performed. Then, the old mask of NDD with PR FEM are adopted to form the different p-buried layer length with boron ion implantation. The p-buried optimum dose of 1×10^{12} cm^{-2} at 210 keV are served as double RESURF conditions [4]. A thick interlevel oxide deposition of TEOS is followed by contact lithography and oxide etching to form the contact window. Finally, metallization and passivation are carried out to complete the LDMOS transistor fabrication sequence.

3. Results and Discussion

Fig. 2 presents the layout design and cross-section of the conventional LDMOS MOSFET. The thickness of gate oxide is 45nm. The width and effective channel length are 20 um and 1.2 um. Fig. 3(a) shows the cross-section FEM-LDMOS with p-buried layer. Fig. 3(b) shows the top-view SEM image of device with maximum NDD PR length. The side wall spacer, gate and PR length can be observed.

Fig. 4 displays the measured off-state characteristic of the new FEM LDMOS transistor with different PR length. The PR length of standard device is served as the reference. The result shows the longer NDD PR length perform the better off-state breakdown voltage. The double RESURF is a effective way to balance the electric field in the NDD region than single RESURF methodology and therefore the breakdown voltage can be improved further. Using NDD-Well PR served as the hard mask of p-buried layer is a better way to reduce the fabrication cost. However, the followed annealing temperature such like silicide or other high temperature processes will result in the dramatically diffusion of p-buried layer toward the channel. The p-buried layer will easily connect with HV p-well to decrease the breakdown voltage. Hence, the PR exposure dose and time control affect the PR length and electrical characteristics further.

Fig. 5 shows the comparison of on-state characteristics of FEM LDMOS with different PR size. The results shows the longer NDD PR length perform the better the on-resistance of the equivalent double RESURF device. The larger p-buried area degrades the on-resistance. The comprehensive comparison of electrical characteristics is summarized in the Table 1. The figure of merit (FOM) (BV /$R_{on,sp}$) is addressed for device efficiency evaluation as well.

4. Conclusion

A new Double RESURF LDMOS device combines with FEM technology has been proposed and successfully demonstrated. The fabricated device of maximum NDD PR size achieves breakdown improvement of 6.3% and has excellent FOM evaluation. Throughout the whole fabrication process, no additional mask is required. Such devices with good off-state breakdown voltage and on-resistance show promising potential in practical applications.

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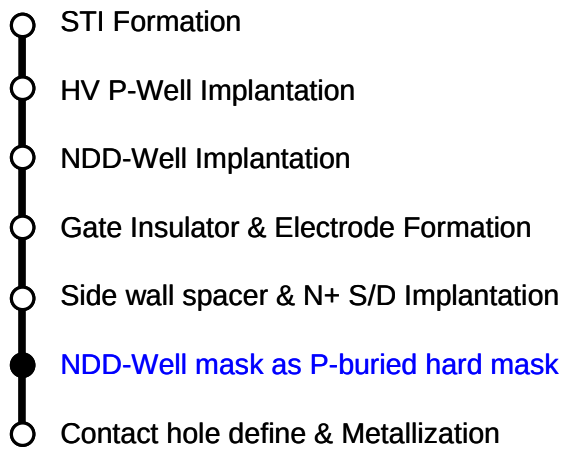

Fig. 1 Fabrication flow of 0.18-um FEM-LDMOS devices.

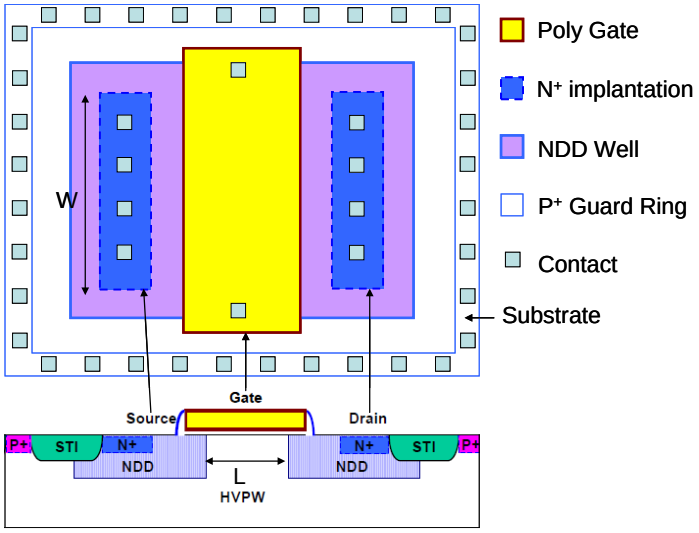

Fig. 2 Layout design and cross-section of the LDMOS MOSFET (W/L=20um/1.2um).

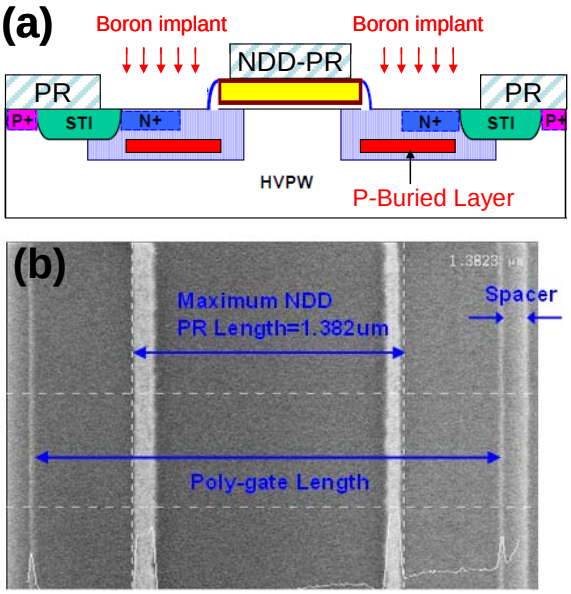

Fig. 3 (a) Cross section LDMOS with p-buried layer.
(b) Top view SEM image of the maximum NDD PR length.

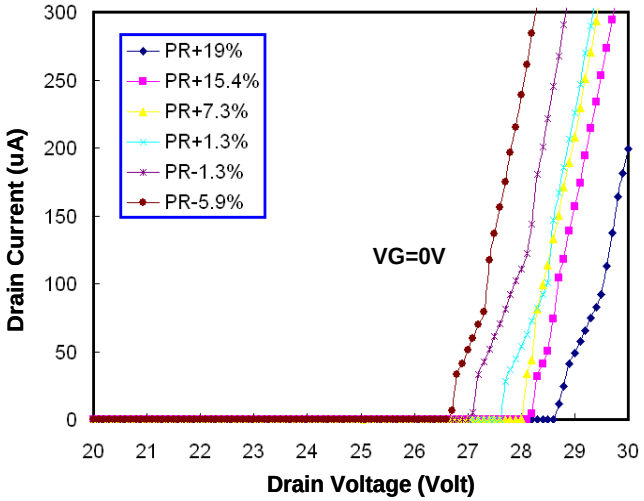

Fig. 4 Measured off-state characteristic of the new FEM-LDMOS transistor with different PR length. The PR length of standard device is served as reference.

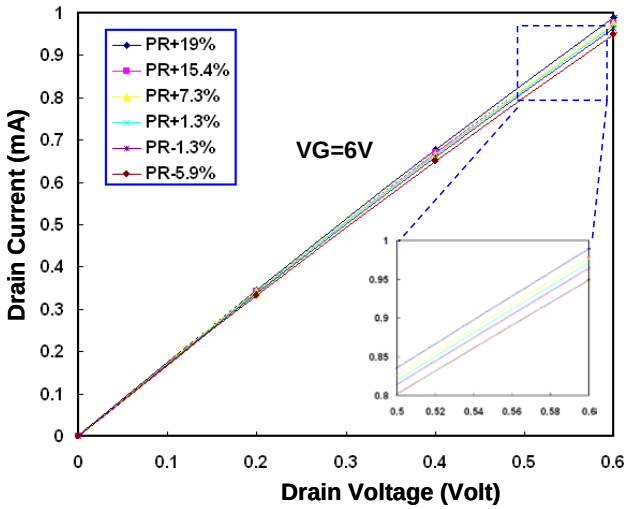

Fig. 5 Comparison of on-state resistance characteristics of double-RESURF LDMOS with different PR size.

LDMOS	NDD-PR Length (um)	$R_{on,sp}$ (mΩ-mm^2) @Vd=0.1V	BV (V) @Ig=1uA	BV%	FOM (BV/$R_{on,sp}$)
PR+19%	1.382	13.89	28.71	6.33	2.07
PR+15.4%	1.320	14.00	28.20	4.44	2.01
PR+7.3%	1.229	13.99	28.00	3.70	2.00
PR+1.3%	1.160	14.09	27.61	2.26	1.96
PR-1.3%	1.126	14.18	27.05	0.19	1.91
PR-5.6%	1.078	14.40	26.61	-1.44	1.85
Conventional	1.145	13.80	27.00	0.00	1.96

Table 1. Summary of different NDD PR size characteristics. The BV and Ron,sp are extracted from forward sweeping Id-Vd curves at Ig=1uA and Vg=6V shown in Figs. 4 and 5. The I-V curve of conventional device is not shown.