

# High Speed Lateral Crystallization of Amorphous Silicon Films on Glass Substrates by Micro-Thermal-Plasma-Jet Irradiation and Its Application to Thin Film Transistor Fabrication

Yuji Fujita, Shohei Hayashi, Hideki Murakami, and Seichiro Higashi

Department of Semiconductor Electronics and Integration Science,  
Graduate School of Advanced Sciences of Matter, Hiroshima University  
1-3-1 Kagamiyama, Higashi-Hiroshima, Hiroshima 739-8530, Japan  
Phone: +81-82-424-7648 Fax: +81-82-422-7038 E-mail: semicon@hiroshima-u.ac.jp

## 1. Introduction

Recently, marked improvement in flat panel displays (FPDs) such as liquid crystal displays (LCDs) and organic light emitting diode (OLED) displays have been achieved based on the development of high-performance thin-film transistors (TFTs). At present, hydrogenated amorphous silicon TFTs are widely utilized to the active matrix backplane of LCDs, however, with the increase in pixel number and frame rate, TFTs with higher mobility are required. For OLED display applications, long term reliability of TFTs under current drive is a crucial issue. Therefore, organic TFTs,<sup>1)</sup> oxide TFTs,<sup>2)</sup> and crystalline-Si TFTs are studied intensively now as the candidates for the next generation TFT channel materials. The crystalline Si TFT has attracted much attention because of their high field effect mobility, high reliability, and its ability to fabricate CMOS circuits.

We have proposed the application of atmospheric pressure discharge micro-thermal-plasma-jet ( $\mu$ -TPJ) to the crystallization of amorphous Si (a-Si) films. One can perform very low cost crystallization because of a very simple structure and high throughput. We have reported that high speed lateral crystallization (HSLC) within microseconds is induced by  $\mu$ -TPJ irradiation to a-Si film on quartz. In HSLC-Si film, we intended to melt Si film and to move the molten region at a very high speed (4000 mm/s), which induce lateral temperature gradient and grain growth to a specific direction. We can confirm dendritic morphology from HSLC-Si films. The maximum grain size was roughly 60  $\mu$ m in length. TFT fabricated by HSLC-Si films showed very high field effect mobility of 350 cm<sup>2</sup>/Vs.<sup>3)</sup> From the view point of industrial applications, we have to further improve two technological matters. First one is to apply HSLC to glass, which is widely used as display substrates. Second one is to control the crystalline growth position and direction, which is quite important to suppress device performance variation.

In this work, we introduced buffer SiO<sub>2</sub> layer to achieve HSLC of a-Si films on glass substrate. We tried to fabricate high performance TFTs on glass. For the position and direction control of grain growth, we introduced Si slit masks.

## 2. Experimental Procedure

After a wet chemical cleaning of glass substrate (Corning Eagle 2000), 0 ~ 600-nm-thick buffer SiO<sub>2</sub> layer were formed on glass substrate by remote plasma enhanced chemical vapor deposition (PECVD) at 300 °C and then 100-nm-thick a-Si films were formed by PECVD using SiH<sub>4</sub> and H<sub>2</sub> at 250 °C. Dehydrogenation was carried out at a substrate temperature of 450 °C in N<sub>2</sub> ambient for 1 hour. The  $\mu$ -TPJ was generated by DC arc discharge under atmospheric pressure with supplying power from 1.2 to 2.2 kW between electrodes. The distance between anode and cathode was 2.0 ~ 3.0 mm. Ar gas flow rate was varied from 7.0 to 9.8 L/min. The  $\mu$ -TPJ was generated by blowing out the arc plasma through an orifice of 0.6 ~ 0.8 mm in diameter. The substrate was linearly

moved by a motion stage in front of the  $\mu$ -TPJ with scanning speed ranging from 1000 to 4000 mm/s. The distance between the plasma source and substrate was 0.8 ~ 1.0 mm.

N-type top gate TFTs were fabricated on glass using  $\mu$ -TPJ crystallized Si films by the following process steps.<sup>4)</sup> Phosphorus doped a-Si film with a thickness of 20 nm was deposited on a 500-nm-thick buffer SiO<sub>2</sub> layer by PECVD and then patterned into islands to form source and drain regions by chemical dry etching (CDE). Intrinsic Non-doped a-Si film with a thickness of 20 nm was deposited on source and drain islands by PECVD at 250 °C. Dehydrogenation was performed at 450 °C in N<sub>2</sub> ambient for 1 hour. The  $\mu$ -TPJ irradiation was performed to crystallize the a-Si film and to activate the phosphorus atoms in source and drain regions, simultaneously. Si layer was then isolated to island shape by CDE. 120-nm-thick gate SiO<sub>2</sub> film was deposited by remote PECVD at 300 °C. Source, drain and gate electrodes were formed by evaporation of Al after opening contact holes by wet etching. The maximum temperature throughout the fabrication process was 450 °C.

In order to control the position and grain growth direction, a slit mask of 0.5 mm in width using 525- $\mu$ m-thick Si wafers was positioned directly on a-Si films during the  $\mu$ -TPJ irradiation (Fig. 1). Scan direction of  $\mu$ -TPJ was perpendicular to the longer direction of the slit.

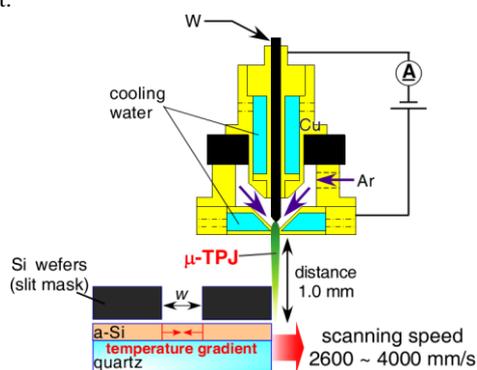


Fig. 1. Schematic diagram of the  $\mu$ -TPJ irradiation to a-Si films with a slit mask of Si wafers.

## 3. Results and Discussion

Many cracks were observed when a-Si film was directly deposited on glass and crystallized by  $\mu$ -TPJ. However, with increasing buffer SiO<sub>2</sub> thickness ( $t_b$ ), cracks markedly decreased. When  $t_b$  is 500 nm, no cracks were observable.

Figure 2(a) shows the Raman scattering spectra of HSLC-Si films with the  $t_b$  ranging from 0 to 553 nm. This result indicates that the HSLC-Si films in all  $t_b$  obtained high-crystallinity comparable to HSLC-Si films on quartz substrate with crystalline volume fraction of almost 100%.

The peak positions obtained from the spectra of Fig. 2(a) are plotted as functions of  $t_b$  in Fig. 2(b). Because glass substrate has

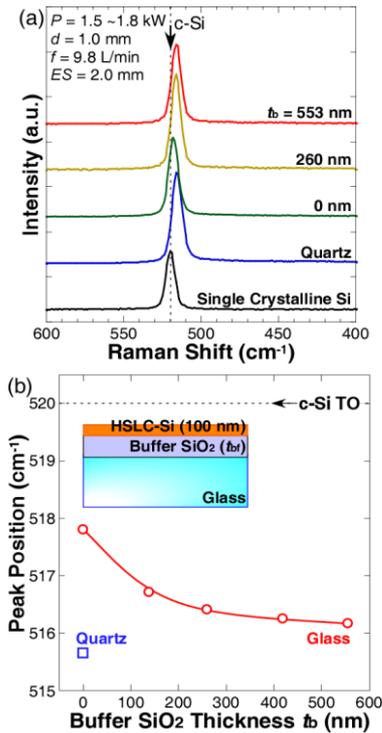


Fig. 2. (a) Raman scattering spectra of HSLC-Si films with the  $t_b$  ranging from 0 to 553 nm and (b) the peak position as functions of  $t_b$ .

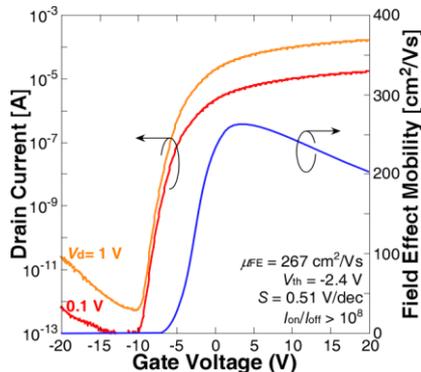


Fig. 3. Transfer characteristics and field effect mobility of HSLC-TFT on glass substrate with 500-nm-thick buffer SiO<sub>2</sub> layer.

larger coefficient of thermal expansion (CTE) than that of quartz, severe thermal stress is generated by temperature gradient near substrate surface. When we use no buffer layer, tensile strain in crystallized Si films is relaxed by formation of many cracks, which results in higher peak position. With increasing  $t_b$ , tensile strain increases with decreasing number of cracks, which suggests that the SiO<sub>2</sub> layer plays a role as strain buffer. In conclusion, we can successfully crystallize a-Si films on glass by introducing ~500 nm buffer SiO<sub>2</sub> layer.

Then, we fabricated TFTs on glass introducing 500-nm-thick buffer SiO<sub>2</sub>. Transfer characteristics of HSLC-TFT on glass substrate are shown in Fig. 3. TFT fabricated by HSLC-Si on glass showed high field effect mobility of 267 cm<sup>2</sup>/Vs. The performance was comparable to that of TFTs fabricated on quartz in the same run.

In order to further improve the TFT performance, we introduced slit mask method. Optical microscope images of HSLC-Si films by  $\mu$ -TPJ irradiation (a) without slit mask and (b) with a slit mask of 0.5 mm in width are shown in Fig. 4. In the case without slit mask, the grain growth direction gradually changes from perpen-

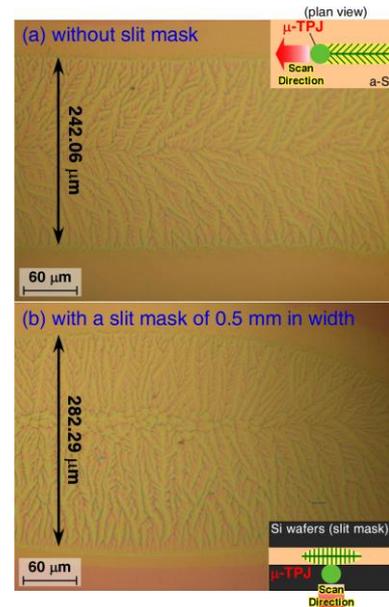


Fig. 4. Optical microscope images of HSLC-Si films by  $\mu$ -TPJ irradiation without slit mask and a slit mask of 0.5 mm in width.

dicular to parallel with respect to the scan direction. However, in the case with a slit mask, the grain growth direction well controlled parallel to the slit width direction. This result suggested that temperature gradient in molten Si was well controlled by the slit mask.

In addition, in the case of using the slit mask, long grain growth of 160  $\mu$ m was confirmed near the center of the slit mask. Because of this result, position and direction of grain growth is very easily controllable by the position of the slit mask.

An additional advantage of slit mask method is to reduce thermal incidence to the glass surface, which is effective to further reduce the thermal strain to glass.

#### 4. Conclusion

We can perform HSLC to a-Si films on glass substrates by  $\mu$ -TPJ irradiation by introducing buffer SiO<sub>2</sub> layer as thick as 500 nm. TFT fabricated by HSLC-Si film on glass with 500-nm-thick buffer SiO<sub>2</sub> layer showed high field effect mobility of 267 cm<sup>2</sup>/Vs.

By positioning the slit mask on a-Si films during the  $\mu$ -TPJ irradiation, it is possible to control the temperature gradient in molten Si and thus grain growth position and direction.

#### 5. Acknowledgements

A part of this work was supported by Research Institute for Nanodevise and Bio Systems, Hiroshima University and Funding Program for Next Generation World-Leading Researchers (NEXT Program) from the Japan Society for the Promotion of Science (JSPS).

#### References

- 1) T. W. Kelley, P. F. Baude, C. Gerlach, D. E. Ender, D. Muyres, M. A. Haase, D. E. Vogel, and S. D. Theiss: Chem. Matter. **16** (2004) 4413.
- 2) D. H. Levy, D. F. Freeman, S. F. Nelson, P. J. Cowdery-Corvan, and L. M. Irving: Appl. Phys. Lett. **92** (2008) 192101.
- 3) S. Hayashi, S. Higashi, H. Murakami, and S. Miyazaki: Appl. Phys. Express **3** (2010) 061401.
- 4) S. Higashi, H. Kaku, T. Okada, H. Murakami, and S. Miyazaki: Jpn. J. Appl. Phys. **45** (2006) 4313