A Compact Nonvolatile Logic Element Using an MTJ/MOS-Hybrid Structure

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1. Introduction

The implementation of a nonvolatile field-programmable gate array (FPGA) [1] is one promising solution for completely eliminating static power dissipation with an instant-on capability [2]. We have presented a nonvolatile lookup table (NVLUT) circuit combining with magnetic tunnel junction (MTJ) devices with MOS transistors [3, 4] which is a fundamental component of a nonvolatile FPGA. It is also necessary to design a nonvolatile logic element (NVLE) which is composed of an NVLUT circuit and a nonvolatile flip-flop (NVFF). This paper presents a compact MTJ/MOS-hybrid NVLE where both the NVLUT circuit and the NVFF are implemented based on a dynamic current-mode logic (DyCML) [5, 6]. Since the low swing signal from an MTJ device can be applied as logic value directly, the proposed NVLE can be implemented compactly. The use of a DyCML also makes it possible high-speed switching operation with low dynamic power. In fact, the proposed 4-input NVLE reduces transistor counts to 55 percent compared to a conventional nonvolatile SRAM (NVSRAM) [7] based implementation. Moreover, the switching delay and the active power of the proposed circuit are reduced to 83 percent and 64 percent with HSPICE simulation under a 90-nm CMOS technology.

2. MTJ/MOS-Hybrid Nonvolatile Logic Element

Figure 1 shows a block diagram of the proposed 2-input NVLE which is composed of a 2-input NVLUT circuit, an NVFF, and a multiplexer (MUX). Any 2-input combinational functions are performed by the NVLUT circuit and sequential functions also can be performed by the combination of the NVLUT circuit and the NVFF.

Figure 2 shows a block diagram of the proposed 2-input NVLUT circuit which is composed of a pre-charged sense amplifier (PCSA) [8], a current selector and a reference current generator. An MTJ device stores data Y as a resistance value; Y=1 corresponds to low resistance RP and Y=0 to high resistance RAP. When EN and CLK are activated at high level, one current path in the current selector is activated according to the complementary inputs (X1, X2') and (X2, X1'), and a current I_X is generated, while a reference current I_REF is generated by the reference current generator. The small difference between I_X and I_REF is sensed and complementary full-swing outputs (D, D') are generated by the PCSA. The MTJ devices in the reference current generator are used to adjust I_REF according to the process variation [4]. MTJ devices in the NVLUT circuit are configured by using word lines and bit lines such as WL0, WL1, BL0 and BL1.

Figure 3 shows a circuit diagram of the proposed NVFF. It consists of an NMOS-based differential-pair circuit (DPC), cross-coupled CMOS inverters, two MTJ devices and MTJ writing circuit. The complementary inputs (D, D') from the NVLUT circuit are stored in the cross-coupled CMOS inverters in the normal operation. They are also stored in MTJ devices (M, M') in the master latch when WCKB is activated at low level.

The behavior of the master latch is explained as follows. Figure 4 (a) shows a THROUGH phase (CLK=1 and CLK'=0). Assume that the voltage at the input node D is VDD and that at D' is 0V. Since M1 and M4 are turned on, the load capacitance Cq is discharged to GND and M6 is turned on. As a result, the load capacitance Cq' is charged and the voltage at the output node q becomes VDD while q' becomes 0V. Figure 4 (b) shows a HOLD phase (CLK=0 and CLK'=1). Since M3 is turned ON, the voltages at the output nodes (q, q') are held in the cross-coupled CMOS inverters. At the same time, M1 and M2 are turned off so that the DPC does not operate. As a result, there is no DC current path from VDD to GND. Figure 4 (c) shows a STORE phase. When the input data (D, D') is (1, 0) and WCKB is activated at low level, M10 and M13 are turned on by NOR gates and write current IW is applied to the MTJ devices. To configure (M, M') simultaneously, the voltage signal Vw is applied to M10 and M11 in the STORE phase. Figure 4 (d) shows a RESTORE phase. When RESB is activated at low level, M9 is turned on and the voltages at q and q' are balanced, and as a result, a clamped voltage is supplied to each MTJ device. Then, the sensing currents I_M and I_M' penetrate through M and M' respectively. When RESB is activated at high level, M9 is turned off and the difference between I_M and I_M' is amplified by the cross-coupled CMOS inverters.

3. Evaluation

A test chip where MTJ devices are stacked over the CMOS logic circuit plane with 90-nm CMOS process has been fabricated. Figure 5 (a) shows a measured R-I curve of the fabricated MTJ device and Fig. 5 (b) shows its measurement environment. Since the total resistance of MOS transistor is 0.18 kΩ in the deep-triode region, R_P and R_SP are 2.60 kΩ and 1.27 kΩ respectively. The performance comparisons between a conventional NVSRAM [7] based 4-input NVLE using a CMOS-based NVFF [9] and the proposed one, are performed by the HSPICE simulation under a 90-nm CMOS technology with the characteristics of the fabricated MTJ device. Table I summarizes the result.
Since the small difference between $I_X$ and $I_{REF}$ can be applied as logic value directly, the sense amplifier is shared in the proposed NVLUT circuit and the number of transistor is greatly reduced. As a result, the proposed NVLE exhibits 45 percent of transistor counts reduction. Moreover, the use of DyCML enables both 17 percent of the switching delay and 36 percent of the active power reduction.

4. Conclusions
A compact MTJ/MOS-hybrid NVLE and its advantages compared to a conventional NVSRAM based implementation are presented. It is important to discuss the relationship between configuration energy and time of the MTJ devices. As future prospect, it is expected that the MTJ/MOS-hybrid FPGA realizes ultra-low power reconfigurable computing.

Acknowledgements
This research is supported by the JSPS through FIRST Program. The authors also wish to thank Noboru Sakimura and Ryusuke Nebashi of NEC, for help in fabrication of the chip.

References