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Comprehensive Understanding of Flatband Voltage Shift Based on Energy Band Alignment of the Whole Metal/high-k/SiO_2/Si Stack

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1. Introduction

The flatband voltage (V_{FB}) tuning is one of the most important issues related to the CMOS device with the high-k/metal gate stack. Several instructive results have been reported for the physical origin of the V_{FB} shift. [1-8]

In this paper, the V_{FB} shift is discussed for the first time based on the energy band alignment of the whole metal/high-k/SiO_2/Si stacks in equilibrium. The thermal equilibriums of the metal/high-k, highi-k/SiO_2 and SiO_2/Si contacts are discussed respectively to establish the equilibrium of the whole stack. The dielectric contact induced gap states (DCIGS) at the metal/high-k and high-k/SiO_2 interfaces are considered to discuss the issue of V_{FB} shift together with the interface or bulk charges of the whole stacks. The positive V_{FB} shift of TiN/HfO_2/SiO_2/Si stack is considered to be attributed to the DCIGS at the TiN/HfO_2 and HfO_2/SiO_2 interfaces. The theoretical calculations are in good agreement with the experimental results.

2. Experimental

All MOS capacitors in this work were fabricated with the process flow shown in Fig. 1. High temperature processes were avoided in order to suppress the structural change or compositional mixing within the whole gate stacks. [3]

3. Results and Discussions

The V_{FB} can be obtained based on the surface band bent of the Si substrate when considering the MOS device with high-k/metal gate structure. High-k dielectric materials and SiO_2 can be thought as semiconductor with wide band gap. Thus the equilibrium of the whole metal/high-k/SiO_2/Si stack can be built based on the equilibriums of the respective metal/high-k, highi-k/SiO_2 and SiO_2/Si contacts. The band alignment of all these contacts can be determined by metal/semiconductor or semiconductor/semiconductor contacts described based on the gap states. [8-14]

The detailed energy band diagram of a metal/high-k/SiO_2/Si stack in equilibrium is shown in Fig. 2. The various physical parameters are defined as follows; the $\phi_{2,L}$, $\phi_{2,R}$, $\phi_{4,L}$, $\phi_{4,R}$ and ϕ_S are the barrier heights measured from the Fermi level to the conduction band minimum for the left side of high-k at the metal/high-k interface, the right side of high-k at the high-k/SiO_2 interface, the left side of SiO_2 at the high-k/SiO_2 interface, the right side of SiO_2 at the SiO_2/Si interface, and the Si substrate, respectively. $D_{2,L}$, $D_{2,R}$ and $D_{4,L}$ are the DCIGS densities of the left and right sides of the high-k, and the left side of SiO_2, respectively. $Q_{2,L}$, $Q_{2,R}$ and $Q_{4,L}$ are the DCIGS charges corresponding to the left side of high-k at the metal/high-k interface, the right side of the high-k at the high-k/SiO_2 interface, and the left side of SiO_2 at the high-k/SiO_2 interface, respectively. Q_3 and Q_5 are the fixed charges at the high-k/SiO_2 interface and SiO_2/Si interface. ρ is the bulk charge density in the high-k dielectric. Q_S is the space charge density of Si substrate. ΔV_1, ΔV_2, ΔV_3, ΔV_4, and ΔV_5 are the potential drops on the gap between metal and high-k, the high-k, the gap between high-k and SiO_2, SiO_2, and the gap between SiO_2 and Si, respectively. ε_0, ε_1, ε_2, ε_3, ε_4, ε_5 and ε_S are the vacuum permittivity, the relative permittivities of the gap between metal and high-k, the high-k, the gap between high-k and SiO_2, SiO_2, the gap between SiO_2 and Si, and the Si, respectively. d_1, d_2, d_3, d_4 and d_5 are the physical thicknesses of the gap between metal and high-k, the high-k, the gap between high-k and SiO_2, SiO_2, and the gap between SiO_2 and Si, respectively. $\phi_{2,CNL}$ and $\phi_{4,CNL}$ are the differences between the charge neutrality level and the valence band maximum for the high-k and SiO_2. $E_{2,g}$ and $E_{4,g}$ are band gaps of the high-k and SiO_2. ϕ_m is the vacuum work function of metal. χ_2, χ_4 and χ_S are the electron affinities of the high-k, SiO_2 and Si, respectively.

There are the following equations for MOS device with metal/high-k/SiO_2/Si stack in equilibrium from the Fig. 2.

$$\phi_m=\Delta V_1+\phi_{2,L}+\chi_2 \quad (1)$$
$$\phi_{2,L}=\Delta V_2+\phi_{2,R} \quad (2)$$
$$\phi_{2,R}+\chi_2=\Delta V_3+\phi_{4,L}+\chi_4 \quad (3)$$
$$\phi_{4,L}=\Delta V_4+\phi_{4,R} \quad (4)$$
$$\phi_{4,R}+\chi_4=\Delta V_5+\phi_S+\chi_S \quad (5)$$
$$\Delta V_1=(ed_1/\varepsilon_0\varepsilon_1)(Q_{2,L}+\rho d_2+Q_{2,R}+Q_3+Q_{4,L}+Q_5+Q_S) \quad (6)$$
$$\Delta V_2=(ed_2/\varepsilon_0\varepsilon_2)(Q_{2,R}+Q_3+Q_{4,L}+Q_5+Q_S+\rho d_2/2) \quad (7)$$
$$\Delta V_3=(ed_3/\varepsilon_0\varepsilon_3)(Q_{4,L}+Q_5+Q_S+Q_3) \quad (8)$$
$$\Delta V_4=(ed_4/\varepsilon_0\varepsilon_4)(Q_5+Q_S) \quad (9)$$
$$\Delta V_5=(ed_5/\varepsilon_0\varepsilon_5)(Q_5+Q_S) \quad (10)$$
$$Q_{2,L}=D_{2,L}(\phi_{2,L}+\phi_{2,CNL}-E_{2,g}) \quad (11)$$
$$Q_{2,R}=D_{2,L}(\phi_{2,R}+\phi_{2,CNL}-E_{2,g}) \quad (12)$$
$$Q_{4,L}=D_{4,L}(\phi_{4,L}+\phi_{4,CNL}-E_{4,g}) \quad (13)$$
$$Q_S=Q_S(\phi_S) \quad (14)$$

The equation (14) means that the areal space charge of Si substrate is the function of band bent of the Si. Based on equations above, the ϕ_S can be obtained for a given stack with the various parameters known. Then the V_{FB} can be

calculated as follows;

$V_{FB}=\phi_S-\Delta E+(eQ_S/\varepsilon_0)(d_1/\varepsilon_1+d_2/\varepsilon_2+d_3/\varepsilon_3+d_4/\varepsilon_4+d_5/\varepsilon_5)$ (15)

where ΔE is the energy difference between the Fermi level and the conduction band minimum of Si substrate far from the SiO_2/Si interface, and it is determined by the doping of Si substrate. Fig. 3 shows the experimental data of the intercepts of the V_{FB}-EOT plots of TiN/HfO_2/terraced SiO_2/Si structure versus five different HfO_2 thicknesses. Also shown in Fig. 3 are the calculation results together with the values of the parameters used in the calculation in order to fit the experimental data. It can be seen that the theoretical results are in good agreement with the experimental data. The slops of the V_{FB}-EOT plots for different HfO_2 thicknesses in experiment are also identical with the simulation which are not shown here. These further demonstrate the feasibility of the proposed theoretical analysis above.

Then the V_{FB} shift is analyzed based on the proposed theoretical calculation. Here the V_{FB} shift is defined as the difference of the intercepts of V_{FB}-EOT curves of the stacks with and without HfO_2. The values of the parameters used in simulation are the same as those above. Fig. 4 shows the V_{FB} shift for three cases; the first case is only considering the effect of the charges at the HfO_2/SiO_2 interface and the bulk charges in the HfO_2 but not considering the DCIGS at the TiN/HfO_2 and HfO_2/SiO_2 interfaces. A negative V_{FB} shift is induced. The second case is only considering the DCIGS at the TiN/HfO_2 and HfO_2/SiO_2 interfaces but not the charges at the HfO_2/SiO_2 interface and the bulk charges in the HfO_2. A positive V_{FB} shift is obtained. The last case is considering both the various charges and the DCIGS, which is the case in Fig. 3. A positive V_{FB} shift is present. It is noted that the V_{FB} shift considering both the charges and DCIGS is not simply the linear addition of the V_{FB} shifts for the case only considering the charges and the case only considering the DCIGS. Thus it can be concluded that the positive V_{FB} shift of the TiN/HfO_2/SiO_2/Si stack relative to the TiN/SiO_2/Si stack is due to the DCIGS at the metal/high-k and high-k/SiO_2 interfaces. The charges transfer between the DCIGS and Si substrate so that the Fermi levels in the Si, SiO_2, HfO_2 and TiN are coincident at thermal equilibrium.

4. Conclusions

The V_{FB} of MOS structure with metal/high-k/SiO_2/Si stack is demonstrated based on the band alignment of the whole gate stack. The positive V_{FB} shift of the TiN/HfO_2/SiO_2/Si stack is attributed to the DCIGS at the TiN/HfO_2 and HfO_2/SiO_2 interfaces. The theoretical calculations are identical with the experimental data.

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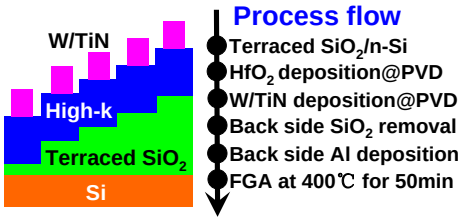

Fig. 1 Schematic diagram of MOS capacitors with a structure of W/TiN/HfO_2/terraced-SiO_2/Si and the process flow.

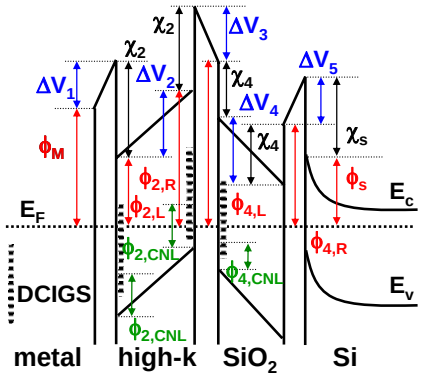

Fig. 2 Schematic diagram of energy band alignment of the MOS device with metal/high-k/SiO_2/Si stack.

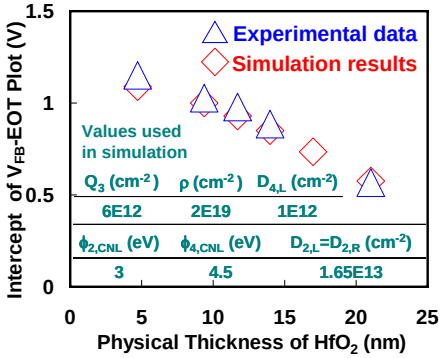

Fig. 3 Experimental data and theoretical calculation results. The values of several physical parameters in simulation are

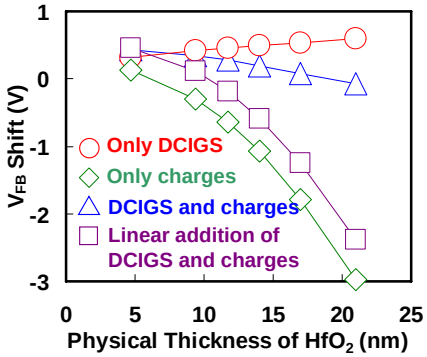

Fig. 4 V_{FB} shifts for the cases only considering the DCIGS, only considering the charges, considering both the DCIGS and charges, and the simply linear addition of the cases of considering the charges only and DCIGS only.