

Lateral Large-Grained Low-Temperature Polycrystalline Silicon-Germanium Thin-Film Transistors on Glass Substrate

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1. Introduction

The use of low-temperature (LT) polycrystalline-silicon (poly-Si) thin film is becoming wide spread in electronic and energy engineering. We have previously reported the fabrication of lateral large-grained (LLG) polycrystalline silicon_{0.95}germanium_{0.05} (poly-Si_{0.95}Ge_{0.05}) films with a grain size of greater than $2 \times 20 \mu\text{m}^2$, on a glass substrate by continuous wave (cw) laser lateral crystallization, using amorphous Si_{0.95}Ge_{0.05} as the precursor.¹⁾ In this study, we evaluated the performance of LLG LT poly-Si_{0.95}Ge_{0.05} TFTs on a glass substrate and carrier scattering mechanism was described. This Ge composition was selected for the following reasons: first, the successful fabrication of poly-Si_{1-x}Ge_x films with grains larger than those of poly-Si has been confirmed at a concentration of Ge = 5% and, second, when using silicon-dioxide (SiO₂) as the gate dielectric, the same TFT fabrication processes used for poly-Si TFTs are applicable due to the low Ge composition.

2. Experiments

An amorphous Si_{0.95}Ge_{0.05} layers with thicknesses of 100 nm were deposited on fused quartz glass using PECVD at a substrate temperature of 300°C. The crystallization was carried out at room temperature using a diode-pumped solid-state (DPSS) cw laser (wavelength = 532 nm) in an air atmosphere after dehydrogenation annealing at 450°C for 60 min. The power instability of the DPSS cw laser was less than 1%, which is superior to that of XeCl excimer and Ar lasers. The glass substrate was transparent to this wavelength. Thus, the laser irradiation did not directly increase the temperature of the glass substrate. The crystallization method described above was developed by one of the authors (A.H.) and is referred to as continuous-wave laser-lateral crystallization (CLC).²⁻⁴⁾ The laser spot size was modulated to a $400 \times 20 \mu\text{m}^2$ ellipsoidal beam using two cylindrical lenses, exhibiting a Gaussian intensity profile. The laser scanning speed was 40 cm/s. An evaluation of the poly-Si_{0.95}Ge_{0.05} crystalline quality was performed by micro-Raman scattering using as-grown films and FE-SEM using Secco etching.

The fabrication processes of the LT poly-Si_{0.95}Ge_{0.05} TFTs are shown in Fig. 1(a). After the formation of transistor islands by RIE, a 50-nm thick gate dielectric SiO₂ film was deposited by applying PECVD and using a SiH₄ + N₂O gas at 325°C. At 300°C, the gate metal Mo was sputtered. To form the S/D regions of n-ch and p-ch LT poly-Si_{0.95}Ge_{0.05} TFTs, the Mo-gate was used as a mask and self-aligned implantation was performed (using 10 KeV with a dose of $2 \times 10^{15} \text{cm}^{-2}$ for phosphorus and 20 KeV with a dose of $2 \times 10^{15} \text{cm}^{-2}$ for BF₂). Then, to activate the dopant, thermal annealing was carried out in nitrogen at 550°C for 6 h. This was the highest process temperature used in our study. After the deposition of a 200-nm thick SiO₂ interlayer, a contact hole was formed by RIE, and Mo was sputtered to form electrodes. Finally, hydrogenation annealing was performed in forming gas at 400°C for 60 min. Figure 1(b) shows a LLG LT poly-Si_{0.95}Ge_{0.05} TFT with $L = W = 10 \mu\text{m}$, in which the SD direction is aligned parallel to the laser scan direction. Reference LLG LT poly-Si TFTs were also fabricated using the same crystallization and device fabrication processes as the ones used for the LLG LT poly-Si_{0.95}Ge_{0.05} TFTs.

3. Experimental Results

Figure 2(a) presents the micro-Raman scattering spectra of the

LLG poly-Si_{0.95}Ge_{0.05} film. This figure illustrates the typical optical phonon mode caused by Si-Si, Si-Ge, and Ge-Ge. Figures 2(b) and (c) show the grains of the poly-Si and poly-Si_{0.95}Ge_{0.05} films. Both were crystallized under the same conditions. It can be clearly observed that the grain size of the poly-Si_{0.95}Ge_{0.05} film is considerably larger than that of the poly-Si film. Grain boundaries are clearly observable at the S/D region in Fig. 1(b). This means the LLG LT poly-Si_{0.95}Ge_{0.05} TFTs contained a lateral large-grained film, as shown in Fig. 2(c).

The transfer characteristics and field-effect mobility calculated from the linear region for both the LLG LT poly-Si_{0.95}Ge_{0.05} TFTs and LLG LT poly-Si TFTs are shown in Fig. 3(a). For the n-ch and p-ch LLG LT poly-Si TFTs, the values achieved for field-effect mobility where 306 and 83 cm²/Vs, respectively. In contrast, the n-ch and p-ch LLG LT poly-Si_{0.95}Ge_{0.05} TFTs achieved field-effect mobility values of only 145 and 42 cm²/Vs, respectively. For the n-ch and p-ch LLG LT poly-Si TFTs, the subthreshold swing-values (s-values) were 240 and 200 mV/dec, respectively, while both the n-ch and p-ch LLG LT poly-Si_{0.95}Ge_{0.05} TFTs had an s-value of 650 mV/dec. Figure 3(b) presents the output characteristic of the LLG LT poly-Si_{0.95}Ge_{0.05} TFTs. Table I contains a summary of the measured LLG LT poly-Si_{0.95}Ge_{0.05} TFTs and LLG LT poly-Si TFTs performances.⁵⁾ In this study, the performances of the LLG LT poly-Si_{0.95}Ge_{0.05} TFTs were inferior to those of the LLG LT poly-Si TFTs. However, the performances of the LLG LT poly-Si_{0.95}Ge_{0.05} TFTs in this study were superior to those previously reported for LT poly-Si_{1-x}Ge_x TFTs with a SiO₂ gate dielectric.⁶⁻¹²⁾

Figure 4 shows the temperature dependency characteristics of the field-effect mobility for n-ch LLG LT poly-Si_{0.95}Ge_{0.05} TFTs. This figure includes the

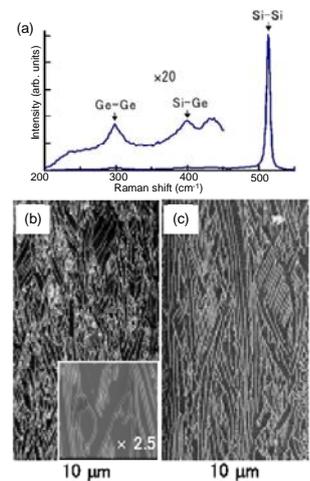


Figure 2. (a) Micro-Raman scattering spectra of lateral large-grained poly-Si_{0.95}Ge_{0.05} film. (b) SEM image of lateral large-grained poly-Si film. (c) SEM image of lateral large-grained poly-Si_{0.95}Ge_{0.05} film.

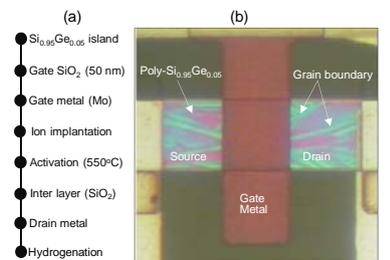


Figure 1. (a) Fabrication processes for poly-Si_{0.95}Ge_{0.05} TFTs. (b) Photograph of fabricated LT poly-Si_{0.95}Ge_{0.05} TFTs with $L = W = 10 \mu\text{m}$.

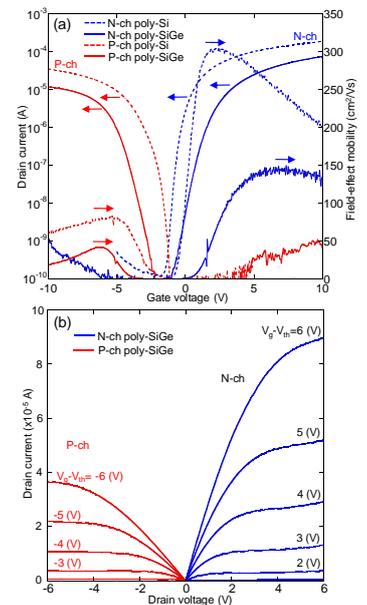


Figure 3. (a) Transfer characteristics of LLG LT poly-Si_{0.95}Ge_{0.05} TFTs and LLG LT poly-Si TFTs. $V_d = 1.0$ and -1.0 (V) for n-ch and p-ch TFTs. The field-effect mobility calculated from linear regions are also shown in this figure. (b) Output characteristic of LLG LT poly-Si_{0.95}Ge_{0.05} TFTs.

Table I. Performance of LLG LT poly-Si_{0.95}Ge_{0.05} TFTs and LLG LT poly-Si TFTs

	Poly-Si _{0.95} Ge _{0.05}		Poly-Si	
	N-ch	P-ch	N-ch	P-ch
Field-effect mobility (cm ² /Vs)	145	42	306	83
S-value (mV/dec)	640	640	240	200

temperature dependency characteristics of the field-effect mobility for n-ch LLG LT poly-Si TFTs, n-ch ELC LT poly-Si TFTs, and n-ch SIMOX-MOSFET fabricated using a low temperature device fabrication processes (LT SIMOX-MOSFET).^{3,4,13} It is noticeable that the temperature dependency characteristics of the field-effect mobility for LLG LT poly-Si_{0.95}Ge_{0.05} TFTs and ELC LT poly-Si TFTs are clearly different. The field-effect mobility for LLG LT poly-Si_{0.95}Ge_{0.05} TFTs decreases monotonically with increasing temperature, similar to the field-effect mobility of LLG LT poly-Si TFTs and LT SIMOX-MOSFET, while the field-effect mobility of ELC LT poly-Si TFTs includes a temperature region exhibiting reverse characteristics.

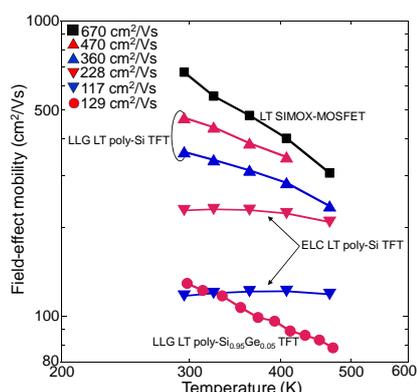


Figure 4. Temperature dependency of the field-effect mobility for n-ch LLG LT poly-Si_{0.95}Ge_{0.05} TFT, n-ch ELC LT poly-Si TFTs, n-ch LLG LT poly-Si TFTs, and n-ch LT SIMOX-MOSFET. The field-effect mobility of each TFTs at room temperature is shown in this figure.

4. Discussion

Growth mechanisms of LLG poly-Si_{0.95}Ge_{0.05} were described in ref.1), thus we briefly summarize it. In order to explain the mechanism for the enlargement of grains in poly-Si_{0.95}Ge_{0.05}, it is important to consider the segregation coefficient of the Ge in molten-Si in addition to the temperature gradient at the solid-liquid interface. It is well documented that in molten Si, the equilibrium segregation coefficient of Ge is 0.33.¹⁴ Therefore, Ge is rejected at the solid-liquid interface. The mechanism for the formation of large-grained poly-Si_{0.95}Ge_{0.05} is attributed to the aggregation of Ge at special sites which are disposed periodically at the solid-liquid interface according to the self-organization mechanism, i.e., the construction of a cellular structure caused by constitutional super-cooling. At low temperatures, the region of Ge aggregation in molten Si_{1-x}Ge_x remains in a molten phase. At this temperature, Ge-lean molten Si_{1-x}Ge_x is transformed into a solid phase. As a result, the solid-liquid interface is automatically stabilized, and the formation of large-grained poly-Si_{0.95}Ge_{0.05} is achieved.

According to our previous research, the dominant carrier scattering mechanism of LT poly-Si TFTs, with a grain size larger than 700 nm and with field-effect mobility larger than 300 cm²/Vs at room temperature, is phonon scattering, rather than grain boundary scattering.¹³ As previously reported in ref. 3 and 4), the carrier scattering mechanism of LLG LT poly-Si TFTs, which are made up of grains much larger than 700 nm, is naturally phonon scattering. The grain size of the LLG LT poly-Si_{0.95}Ge_{0.05} film was larger than that of a LLG LT poly-Si film. Thus, it is thought that phonon scattering, and not grain boundary scattering, is the dominant carrier scattering mechanism in the LLG LT poly-Si_{0.95}Ge_{0.05} TFTs. The results presented in Fig. 4 support this view. Figure 4 shows the temperature dependency of the field-effect mobility for LLG LT poly-Si_{0.95}Ge_{0.05} TFTs to be proportional to T^{-1.1} for n-ch. In Fig. 4, the thermally activated carrier transport region appears in the temperature region below 400 K for ELC LT poly-Si TFTs. This behavior is due to the fact that the ELC LT poly-Si TFTs are made up of small grains, with grain sizes in the range of 200–400 nm, which it turn result in field-effect mobility values lower than 300 cm²/Vs. While, LLG LT poly-Si_{0.95}Ge_{0.05} TFTs include very large grains, with sizes greater than 2 × 20 μm², grain boundary scattering is negligible. Therefore, the temperature dependency of the field-effect mobility indicates a phonon scattering mechanism.

To explain the degradation of the field-effect mobility for the LLG LT poly-Si_{0.95}Ge_{0.05} TFTs compared to that of LLG LT poly-Si TFTs, another scattering mechanism is required. According to previous Hall effect measurements, the mobility of bulk Si_{1-x}Ge_x is lower than that of pure-Si and pure-Ge. This is thought to be caused by alloy scattering.¹⁵ Also in this research, alloy scattering will be thought to be one of mechanism which explains why the field-effect

mobility values for the LLG LT poly-Si_{0.95}Ge_{0.05} TFTs were lower than those of the LLG LT poly-Si TFTs, in spite of the larger grains in the poly-Si_{0.95}Ge_{0.05} compared to those of poly-Si. Reference 16) and 17) showed that temperature dependency of field-effect mobility due to alloy scattering is proportional to T^{-1/2}. Since field-effect mobility of n-ch LLG LT poly-Si_{0.95}Ge_{0.05} TFT shows T^{-1.1} temperature dependency, thus effect of alloy scattering is not dominant. This is consistent with low Ge concentration of 5%.

In addition to weak effect of alloy scattering, the inferior quality of poly-Si_{0.95}Ge_{0.05}/SiO₂ interface is another effect for degradation of field-effect mobility of LLG LT poly-Si_{0.95}Ge_{0.05} TFTs. The s-values of the LLG LT poly-Si_{0.95}Ge_{0.05} TFTs are larger than those of the LLG LT poly-Si TFTs. This indicates that the quality of the poly-Si_{0.95}Ge_{0.05}/SiO₂ interface is much poorer for the LLG LT poly-Si_{0.95}Ge_{0.05} TFTs than that for the LLG LT poly-Si TFTs. This is also a degradation mechanism of the field-effect mobility for LLG LT poly-Si_{0.95}Ge_{0.05} TFTs. This may be caused by insufficient hydrogenation of the Ge dangling bond at the poly-Si_{0.95}Ge_{0.05}/SiO₂ interface. Therefore, it will be necessary to optimize the hydrogenation of the Ge dangling bond to improve both the field-effect mobility and s-values for LLG LT poly-Si_{0.95}Ge_{0.05} TFTs.

Although the field-effect mobility for the LLG LT poly-Si_{0.95}Ge_{0.05} TFTs was lower than that of the poly-Si TFTs, it was sufficient to achieve a SOG when applied to an AMLCD's and an AMOLED's peripheral circuit. Furthermore, the low melting temperature of Si_{1-x}Ge_x, compared to that of Si, is a beneficial characteristic that will make it possible to reduce the thermal damage to a glass substrate during the crystallization process.

5. Summary

In summary, we fabricated LLG LT poly-Si_{0.95}Ge_{0.05} TFTs on glass substrates at a low process temperature of 550°C using a SiO₂ gate dielectric and obtained field-effect mobility values of 145 and 42 cm²/Vs for n-ch and p-ch TFTs, respectively. These values are better than the previously reported LT poly-Si_{1-x}Ge_x TFTs values obtained using a SiO₂ gate dielectric. However, they are worse than those of the LLG LT poly-Si TFTs. This result holds true, in spite the fact that larger grain was formed in LLG poly-Si_{0.95}Ge_{0.05} than in LLG poly-Si. Temperature dependency of field-effect mobility of LLG LT poly-Si_{0.95}Ge_{0.05} TFTs indicates phonon scattering mechanism. This indicates effect of alloy scattering is weak. While, according to inferior subthreshold values of LLG LT poly-Si_{0.95}Ge_{0.05} TFTs, the quality of the poly-Si_{0.95}Ge_{0.05}/gate-SiO₂ interface was found to be poor. Thus, optimization of interface state, including hydrogenation of Ge at poly-Si_{0.95}Ge_{0.05}/gate-SiO₂, is necessary to improve both field-effect mobility and subthreshold swing. Although the field-effect mobility of the LLG LT poly-Si_{0.95}Ge_{0.05} TFTs is lower than that of the poly-Si TFTs, it is sufficient to achieve SOG when applied to AMLCD and AMOLED peripheral circuits. Furthermore, the low melting temperature of poly-Si_{1-x}Ge_x is a beneficial characteristic that is expected to reduce the damage to a glass substrate during the crystallization process.

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