Extended Abstracts of the 2011 International Conference on Solid State Devices and Materials, Nagoya, 2011, pp38-39

Electrical Characteristics of Back Gated FET on a Wrinkle Free Graphene Channel

Chun Hum Cho[1], Sung Kwan Lim[1], Chang Goo Kang[2], Young Gon Lee[2],
Hyeon Jun Hwang[2], Eunji Park[1], and Byoung Hun Lee[1, 2]

[1]Department of Nanobio Materials and Electronics, [2]School of Materials Science and Engineering
Gwangju Institute of Science and Technology, 1 Oryong-dong, Buk-gu, Gwangju, Korea 500-712
Phone: +82-62-715-2308, E-mail: bhl@gist.ac.kr

1. Introduction

Graphene is an attractive material for high performance transistor application [1-4, 9]. In order to implement graphene FETs, a wafer scale graphene process is necessary. However, current epitaxial or CVD graphene processes require very high temperature ranging from 700 ^{o}C -1400 ^{o}C, which is not compatible with CMOS process. Moreover, difference in thermal expansion coefficients between a template and graphene causes wrinkle defects [3, 4].

Thus, a low heat cycle graphene process using a pulsed excimer laser anneal (25nsec, 248nm KrF laser) has been proposed to make a wrinkle free graphene [5, 6]. Since the penetration depth of 25 nsec pulsed KrF laser on the SiC wafer is less than 100 nm and thermal impacts of anneal propagates much less than 4 um depth, a localized graphene growth is feasible with a laser anneal. Also, wrinkle defects can be avoided due to relatively shallow depth of the thermally activated region. Recently, two groups have reported laser graphitization processes on 4H-SiC. However, electrical properties of the graphene FET with laser graphitization process have not been reported [5, 6]. In this work, physical and electrical properties of graphene grown by the laser graphitization have been reported.

2. Experiments

In this work, Si-faced 4H-SiC wafer was used to be graphitized by pulsed KrF laser in high vacuum (<5 x 10^{-7} Torr). The quality of the graphene on the graphitized SiC was analyzed by SEM, AFM and Raman spectroscopy (Renishaw, 514 nm).

In order to fabricate graphene FETs with a back gate, the transfer process from laser annealed SiC onto SiO_2 was carried out. For the transfer process, 90 nm SiO_2 as target substrate was treated using O_2 plasma to improve adhesion between graphene and the substrate followed by acetone, methanol and D.I. sonication. After 100 nm of Au films was deposited on the graphitized SiC using an e-beam evaporator, thermal release tape (Revalpha, Nitto Denko) was introduced as a supporting material on the Au/graphene/SiC stack to detached graphene from the graphitized SiC. Then, the stack of tape/Au/graphene was transferred to SiO_2 substrate. In order to remove the tape and Au, the sample was heated at 130 ^{o}C on a hot plate and etched in a gold etchant respectively.

The transferred graphene on 90 nm SiO_2 was patterned using a photolithography and O_2 plasma etching. 50 nm Au electrode was defined using an e-beam evaporator and lift-off. Then, an ALD Al_2O_3 capping layer to reduce p-doping effect[7] was deposited on top of the graphene channel at 130 ^{o}C. Then, a back gate electrode (50 nm Ni) was deposited on backside of the SiO_2/Si wafer using a RF magnetron sputter followed by removing native oxide of Si.

Finally, back gated graphene FETs were characterized using a parameter analyzer (Keithley 4200).

3. Physical analysis of graphene

After the graphitization process, graphene seems to be formed on bright area with about 2 x 2 mm^2 area on the SiC surface as shown in Fig.1(a). Typically, a more conductive material has brighter contrast. Fig.1(b) shows AFM image of graphene on graphitized SiC. There is wrinkle free graphene surface within 30 x 30 um^2 area.

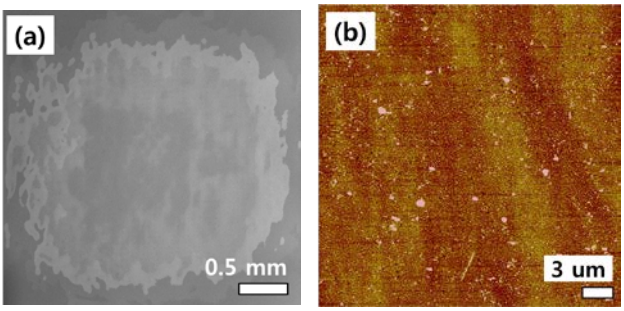

Fig. 1 (a) SEM and (b) AFM image
of epitaxial graphene on the graphitized 4H-SiC.

Raman analysis was carried out on two kinds of area, the center and the side area as shown in Fig. 2. Raman spectra of each area indicate high D peak intensity implying atomic structural defects of the graphene. We expected that a rapid heating and cooling cycle of the laser anneal resulted in the high D peak. Particularly, the Raman spectrum of the center area has higher D/G peak ratio (~0.57) than the side area (~0.35), as well as, the thickness of the graphene at the center is thicker than that of the side according to G/2D peak ratio (center: 0.77, side: 0.56) and FWHM of 2D peak (center: 64 cm^{-1}, side: 22 cm^{-1})[6, 8]. These results indicated different conditions of thermal activation between two areas and the condition of the center area seems to be tougher than the side area. Although, homogenized laser beam affected on the SiC wafer, cooling rate of the side area was higher than the center because the side area was adjacent to the area on the outside of the laser beam.

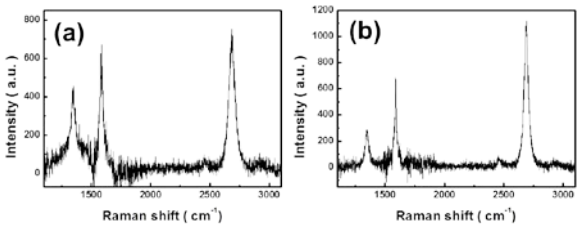

Fig. 2 Raman spectra of graphitized SiC ; (a) center area and (b) side area.

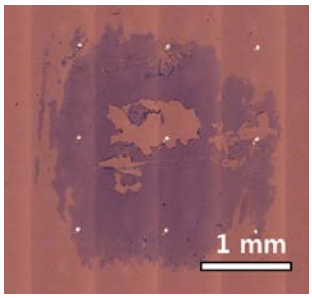

Fig. 4 Optical image of the transferred graphene on SiO_2

After transfer process, the area of the transferred graphene on SiO_2 was suitable to fabricate transistor using a photolithography although some area of the graphene was lost as shown in Fig. 4. Then, back-gated graphene FETs were fabricated using the process as described in the experiments section.

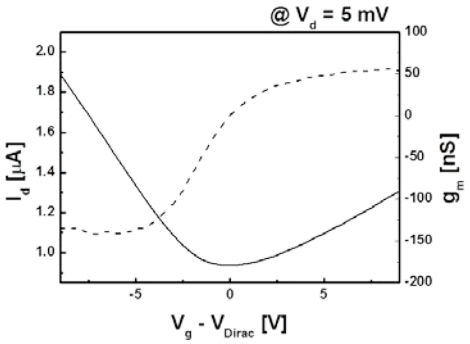

Fig. 5 I_d-V_g curve and transconductance of the graphene FET at the center area.

Fig. 5 shows the I_d-V_g curve and transconductance of the graphene FET at the center area. In the I_d-V_g curve, Dirac point was clearly observed even it had a few layer graphene. The result is a consequence for non-Bernal structure induced by the rapid heat cycle of laser process. When graphene is exposed in air, it is often doped as p-type by water related molecules. An ALD process for Al_2O_3 capping layer was found to reduce the doping effect by the self-cleaning effect of the process and isolating the graphene from air. Introducing the Al_2O_3 capping layer, symmetrical I_d-V_g curve were obtained as shown in Fig. 5.

Field effect mobility of 40 back-gated graphene FETs was estimated. The best hole and electron mobility were 702 cm^2/Vs and 873 cm^2/Vs, respectively. These values are lower than other devices with thermally graphitized 4H-SiC reported recently[9]. For our work, we predicted that wrinkle free morphology of graphene would be dramatically improved due to wrinkle free morphology of the graphene reducing the scattering of the charge carrier. However, the mobility is lower than Ref. 9 because of the atomic structural defect. The distribution of the mobility was mapped as shown Fig. 6. Although some part of the center area was lost when transfer process, the mapping image indicated different mobility depending on area. The side area has higher mobility than the center, which appears to be related to the thickness of graphene and D/G ratio indicating the structural defect. Moreover, since variation of device performance would negatively affect device integration for COMS process, the laser graphitization process should be more carefully studied to growth uniform graphene.

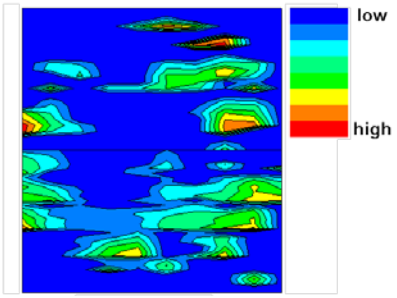

Fig. 6 Mapping image of the field effect mobility distribution on the whole area.

3. Conclusions

Wrinkle free graphene has been successfully grown by a laser graphitization on 4H-SiC. 40 back gated graphene FETs have been well fabricated, however, the best field effect mobility was lower than another. Moreover, there is the variation of device performance depending on the property of graphene on each area. Therefore, further study of the laser graphitization process for uniform graphene should be necessary as well as high quality graphene.

Acknowledgements

This work was supported by the world class university program and mid-carrier researcher program through National Research Foundation (NRF) grant funded by the Korea government (MEST) (No. 2010- 0019122, R31-10026)

References

[1] J. Kedzierski et al., IEEE Trans. Elec. Dev. **55**(8), p.2078 (2008)
[2] J.S. Moon et al., IEEE Elec. Dev. Lett. **30**(6), p.650 (2009)
[3] Luxmi et al., Appl. Phys. Lett. **95**, 073101 (2009)
[4] G. Prakash et al., Carbon, **48**, p.2383 (2010)
[5] S.K. Lim et al., Ext. Abs. of SSDM, pp.591 (2010)
[6] S.W. Lee et al., ACS Nano, **4**(12), p.7524 (2011)
[7] Y.G. Lee et al., Ext. Abs. of IWDTF, pp.21 (2011)
[8] D.S. Lee et al., Nano Lett., **8**(12), p.4320 (2008)
[9] J.S. Moon et al., IEEE Elec. Dev. Lett. **31**(4), p.260 (2010)