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Formation of Ohmic Contacts with Shallow NiGe/n$^+$ Ge Junction

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1. Introduction

Ge is regarded as a strong candidate for realizing high-speed MOSFETs [1] or infra-red photodetectors (PDs) [2], thanks to its superior properties compared to Si, i.e., higher mobiliteis of holes and electrons, and efficient light absorption in the wavelength range around 1.55 μm. However, quite a large contact resistance of metal/n$^+$Ge junction exists as a technology barrier, which is caused by the poor dopant activation in n$^+$Ge [3], and Fermi level pinning effect at the interface[4]. Moreover, a large impurity diffusion in n-Ge [3] makes it difficult to form shallow metal/n$^+$Ge junctions needed for above devices. So far, several methods to overcome these problems have been proposed [5-7]. Nishimura *et al*. [5] utilized “snowplow” effect during nickel germanide (NiGe) formation, in which impurities segregate towards the NiGe/n$^+$Ge junction and reported such junction shows ohmic contact realized by the increased tunneling current. This paper focuses on further lowering of the resistance in metal/n$^+$Ge junction, aiming at high-speed PD applications. We used the NiGe process, and applying an activation annealing prior to the NiGe formation.

2. Experiments

In the series of experiments, we have used 1 μm Ge epitaxial layers grown on Si substrate, so as to reproduce the same condition as that of the Ge PDs. Phosphorus (P) ions were implanted in the Ge layer with various energies which were tuned so as to place the impurity peak in the range of 5 to 50 nm from the surface. After the implantation, rapid thermal annealing (RTA) was performed at 500 to 600 ˚C for 10 to 60 s. Patterned SiO_2 was subsequently formed on the Ge, and NiGe was selectively formed in the opening window, by using Ni sputtering and successive germanidation annealing (400 ˚C, 30 s). The contact resistance was evaluated with using the Kervin pattern, and the value was defined in J-V characteristics around 0 V.

3. Results

Figure 1 shows the J-V characteristics of the samples with various ion implantation energies and annealing conditions. P implanted sample with lower energy (E1) shows the rectified J-V characteristics, indicating the presence of Fermi level pinning which is characteristic feature of metal/n-Ge junction. On the other hand, samples implanted with higher energy (E2) P show ohmic J-V characteristics, and contact resistances of these samples are as low as 3.2×10^{-5} Ω·cm^2. The ohmic characteristics are attributed to an increase of tunneling currents, suggesting the existence of high density activated carriers at the NiGe/n$^+$Ge junction. Here, note that the samples implanted with the energy E2 have almost the same contact resistances irrespective of the annealing temperatures.

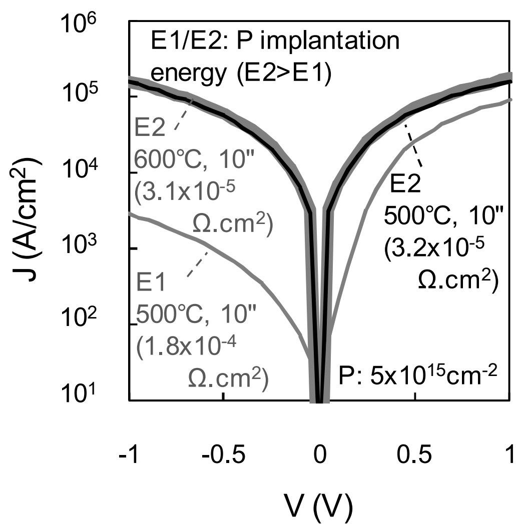

Fig. 1 Current density-voltage (J-V) characteristics of the NiGe/n$^+$Ge samples with various P implantation and activation annealing conditions.

The SIMS profiles and corresponding TEM image of these samples are shown in Fig. 2. Samples with higher implantation energy (E2) have impurity densities at NiGe/n$^+$Ge junction higher than that of the sample with lower implantation energy (E1) by almost an order of magnitude, which explains the prominent reduction of the contact resistance shown in Fig. 1. In addition, it is noteworthy that the impurity densities at NiGe/n$^+$Ge junctions between these two samples coincide each other, in spite of the difference of the annealing temperature. The above tendency corresponds well to the results of J-V characteristics in which these samples show the same value of the contact resistance, indicating that the contact resistance is determined only by the impurity density at NiGe/n^+Ge junction and the impurity profile in the Ge layer has little effect on the contact resistance. Here, the sheet resistance has shown that the carrier activation before the NiGe formation was lower in the sample annealed at 500 ˚C than the sample annealed at 600 ˚C. Therefore, the NiGe formation is found to be an indispensable technique to activate carriers at low thermal budget.

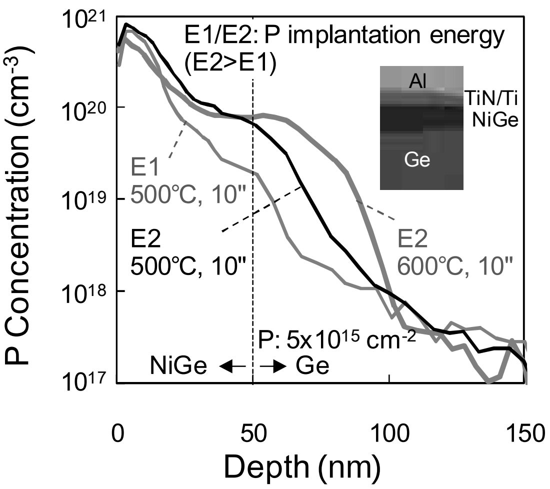

Fig. 2 SIMS profiles of the NiGe/n^+Ge samples with various P implantation and activation annealing conditions.

Figure 3 shows the bench mark of contact resistances of metal/n^+Ge junction as a function of the thermal budgets. Nishimura, *et al.* [5] firstly applied the germanidation process to lower the contact resistance, although obtained contact resistance is still high from a viewpoint of practical applications.

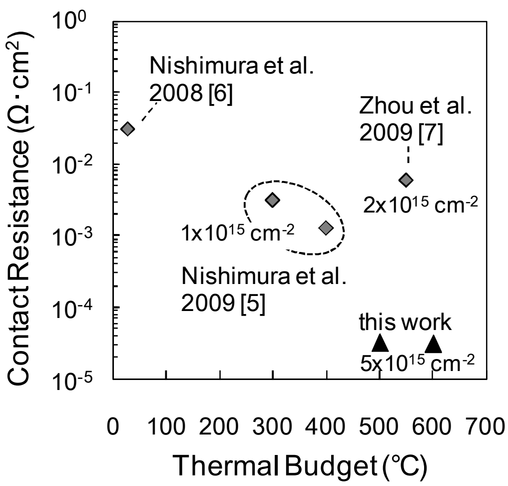

Fig. 3 Benchmark of the contact resistances of metal/n^+Ge junction as a function of the thermal budgets during the process.

In this study, by inserting the activation annealing, we have shown a drastic lowering of the contact resistance (~ 1/100 of the Nishimura's data). The obtained values are sufficient for device applications. As for the physical origin of such resistance reduction, we think the recrystallization before the metal-induced crystallization (MIC) might increase the probability of P capturing to the substitutional site during the MIC. From the J-V characteristics and the SIMS profiles, we estimate that almost $1x10^{20}$ cm^{-3} of carriers are activated at NiGe/n^+Ge junction, which is almost an order higher than the previously reported NiGe process without activation annealing [8]. The activation annealing, however, was found to lower the effect of the "snowplow" effect compared to the NiGe formation without the activation annealing [8]. Hence, we think that the tuning of the implantation energy becomes important in this process, in order to achieve quite a low contact resistance.

3. Conclusions

In the study of metal/n^+Ge junction process, we have concluded there exist two important process conditions for realizing low contact resistance at low thermal budget. First, the necessity of NiGe formation process was confirmed in order to lower the process temperature. Second, tuning of the P implantation energy and the insertion of the activation annealing prior to the NiGe formation were found to be important for lowering the contact resistance. As a consequence, we have achieved the contact resistance as low as $3.2x10^{-5}$ $\Omega\cdot cm^2$, while lowering the thermal budget from 600 ˚C to 500 ˚C. We think that the obtained values are sufficient for device applications such as high-speed Ge PDs.

Acknowledgements

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