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Thermal Stability of Single and Alloy Noble Metals as for PMOS Gate Electrode

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1. Introduction

High-k/metal gate (HKMG) was successfully implemented to 45nm and 32nm technology for some applications [1]. Recently, its application was expanded to even 3D transistor such as Tri-gate for next 22nm technology. However, there are still several concerns such as thermal and electrical instability of threshold voltage (V_{th}), especially for p type metal-oxide-semiconductor (PMOS) devices. This V_{th} instability drives two different integration schemes called gate-first (GF) and gate last (GL). In order to reduce V_{th}, low and high work function (WF) metal gates are needed for NMOS and PMOS device, respectively. Noble metals known as high WF materials had been investigated for PMOS MG gate candidate, but could not maintain high WF. Also, there are few reports to understand WF lowering with thermal budgets in noble metals [2].

In this study, thermal and electrical stability of single noble metals (Pt, Ir, Pd), alloy (IrPt) and control TiN gate electrodes was investigated with atomic layer deposited (ALD) HfO_2 MOS capacitor. Flatband voltage (V_{FB}) of e-beam evaporated single metal and sputtered TiN gated devices substantially shift toward mid-gap position while alloy case shows suppressed thermal-induced V_{FB} shift upon various annealing temperatures. It is attributed to oxygen diffusion into interfacial layer (IL) between Si and HfO_2, leading to thicker IL and vacancy generation in dielectric.

2. Experiment

ALD HfO_2 was deposited on pre-cleaned Si using TEMA-Hf and H_2O oxidant at 300℃. Various noble metals (Ir,Pt, Pd, IrPt) were prepared by e-beam evaporation, followed by sputtered TiN capping deposition. Control TiN was also attained by DC-sputtering. After patterning, forming gas anneal (FGA) was carried out at various temperature range (350℃~450℃) for 30min. Some samples received additional 1000℃ rapid thermal anneal (RTA). Electrical and physical characterizations were carried out to evaluate thermal and electrical stability depending on metals and FGA temperatures

3. Results and Discussion

Figure 1 shows C-V behaviors for single noble metals (Pt, Ir, Pd) MOS capacitors before/after FGA (450℃, 30m). All as-prepared noble metals exhibit high effective WF, while they become midgap-like characteristics after anneal. Amount of V_{FB} shift and increased electrical oxide thickness (EOT) in Pt gate are substantial compared to other metals. Electrons caused by oxygen vacancy generation in HfO_2 are given up to metal gates, leading to lower metal gate WF with increased IL between Si and HfO_2 [3]. Figure 2 also shows TiN MOS device has a similar thermal instability with increasing FGA temperature. As-deposited TiN sample shows higher EWF than midgap characteristic, but starts to lose EWF. Additional high temperature annealing similar to source/drain (S/D) activation step loses EWF further. IrPt shows improved thermal stability compared to other single noble metal and TiN as shown in fig 3. Its EWF is almost 4.9~5.0eV even after 450℃ FGA. Figure 4 shows IrPt has 270mV higher V_{FB} than TiN with 450℃ FGA. For IrPt sample, IL becomes thicker by 0.17nm after 400℃ anneal, but annealed IrPt sample shows thinner IL than that of single Pt sample as shown in Fig 5. Fig 6 shows the correlation between V_{FB} and IL thickness attained from transmission electron microscopy (TEM) analysis. It is observed that lower V_{FB} is attained with thicker IL. It can be attributed to more oxygen diffusion from HfO_2 into Si interface, leading to thicker IL and corresponding oxygen vacancy generation in HfO_2 depending on metal gates. IrPt suppresses to activate thermal-induced vacancy formation in HfO_2 due to modified crystal structure. IrPt/HfO_2 barrier height (Φ_B) was extracted using tunneling current method [4]. Higher FGA temperature reduces Φ_B. 450℃ FGA causes IrPt work-function to lower 320 mV and increase fixed charge density (ΔN_f) by $4.2x10^{11}cm^{-2}$ considering V_{FB} shift as shown in fig 7. Figure 8 shows dependence of IrPt work function on FGA temperatures. IrPt exhibits substantial enhanced electrical stability. It still shows high 4.95eV work function even after 450℃ FGA for 30min.

4. Conclusion

Thermal stability of single (Pt, Ir, Pd) and alloying noble metals (IrPt) was studied. Compared to single metals, alloy shows improved thermal stability. This is attributed to less oxygen diffusion to Si IL, consistent to TEM results due to modified metal gate structure. As a result, lower oxygen vacancy generation is expected into HfO_2, keeping high WF.

Acknowledgements

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References

[1] P. Packan et al., International Electron Devices Meeting (IEDM), (2009) 659

[2] E. Cartier et al., Symposium on VLSI Technology (VLSI), (2009), 42

[3] C.Choi et al., Appl. Phys. Lett. 98 (2011) 123506

[4] S. Zafar et al., Appl. Phys. Lett. 80 (2002) 4858

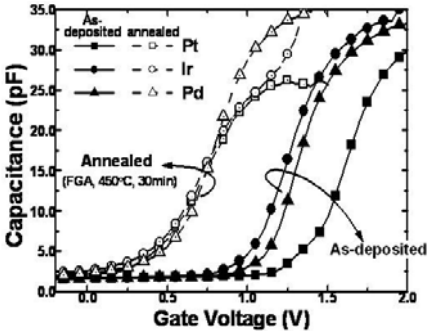

Fig. 1 C-V behaviors for various single noble before/after FGA (450°C, 30min).

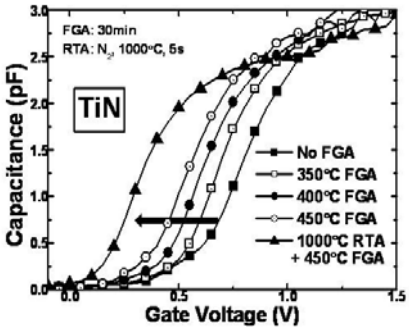

Fig. 2 C-V results with TiN MOS capacitors with FGA temperatures.

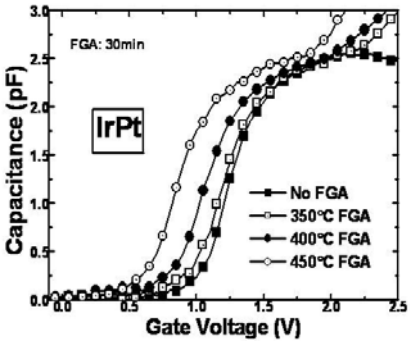

Fig. 3 C-V behaviors with alloying noble metals for various FGA conditions.

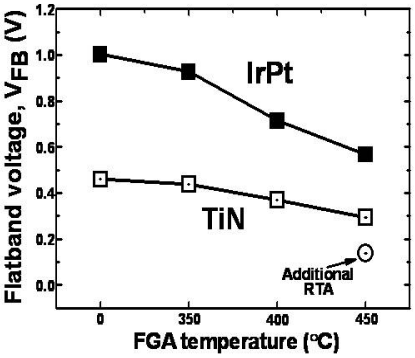

Fig. 4 V_{FB} shifts for IrPt and TiN for different conditions.

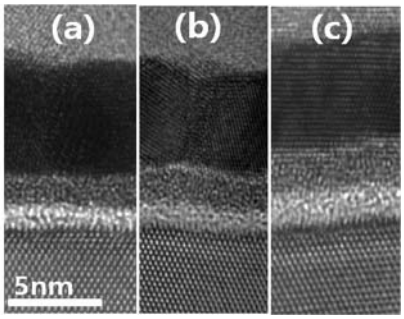

Fig. 5 TEM images for (a) as-deposited IrPt, (b) annealed IrPt, (c) annealed Pt. FGA was done with 400C, 3min.

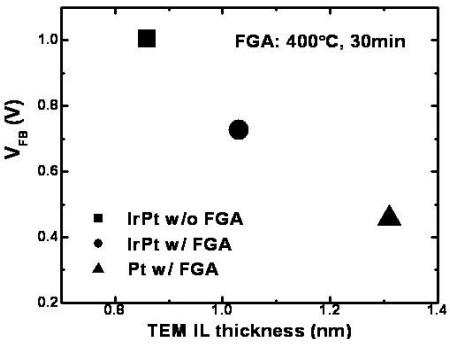

Fig. 6 TEM IL and V_{FB} for IrPt and Pt samples.

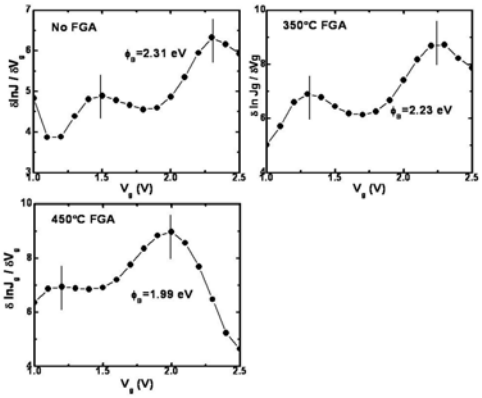

Fig. 7 Barrier heights of IrPt samples under several conditions.

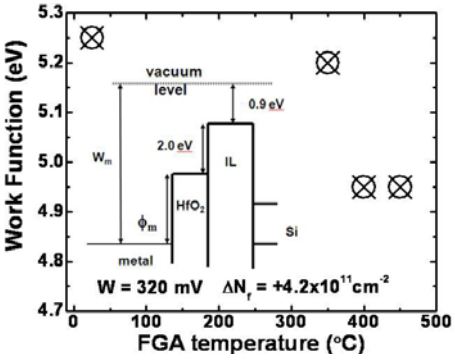

Fig. 8 WF for IrPt samples as a function of FGA temperature.