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Fullerene Memory Transistors with a Chargeable Polymer

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1. Introduction

In conventional organic memory transistors, metals[1,2] and nanoparticles[3,4] have been widely used as charge storage materials. That requires using vacuum evaporation process to fabricate them.[1-4] Furthermore, these inorganic materials are not convenient for low manufacturing cost, and low temperature processes. Recently, chargeable polymers such as poly(α-methylstyrene)[5] and poly(9,9-dioctylfluorene)[6] were demonstrated as substituted candidates in memory transistors. However, the attempt of this approach is still underdeveloped. Additionally, the drawback of these structures is that electron movements through pentacene semiconductor in programming/erasing (P/E) operations require as high as 100 V.[7] Fullerene (C60) has been widely utilized as electron transfer materials in organic electronics.[8] This work introduces organic memories using thin films of poly-perfluoro-alkenyl vinyl ether (CYTOP) as electron storage media embbeded in C60 transistors. The memory devices can be programmed/erased by applying gate pulses of 50/-45 V. The retention time characteristics indicate stable memory devices.

2. Experimental

The devices were fabricated on a heavily doped Si wafer (n+Si, resistivity: 1-100 Ωcm) as a gate electrode, where SiO_2 served as a dielectric layer (Fig. 1(a)). A chargeable layer of CYTOP (CTL-809M, Asahi Glass) was spin-coating onto the gate dielectric and dried at 100 ^{o}C for 2 h. A thin film of C60 was grown by thermal evaporation at a deposition rate of 0.1 nm s^{-1}. Al source-drain electrodes were finally formed at a deposition rate of 0.3 nm s^{-1} (channel length (*W*)= 2 mm, channel width *(L)*= 50 μm). Electrical measurements of the transistors were done using a Keithley 4200 semiconductor characterization system at room temperature.

3. Results and discussion

The transfer (Fig. 1(b)) and output (Fig. 1(c)) characterisitics of the transistors exhibited a *n*-channel field-effect properties in the operation region of positive gate voltage (V_G). The threshold voltage (V_{Th}), electron mobility (μ), subthreshold slope (S), and on/off current ratio were 2.8 V, $4x10^{-1}$ cm^2 V^{-1} s^{-1}, 900 mV/decade, and $0.6x10^5$, respectively. In general, the *n*-type transistors showed good parameters under low-voltage operation.

The programmable characteristics of the memory devices are shown in Fig. 2(a). The transfer curve shifted after applying a gate voltage of 50 V for 100 ms (program). And then, by applying a reverse gate voltage of -45 V for 100 ms (erase), the transfer curve come back the initial position. The V_{Th} changed from 2.8 to 12.8 V, resulting in a memory window (ΔV_{Th}) of 10 V (Fig. 2(b)). Clearly, the obtained ΔV_{Th} indicates a memory effect realized in the devices.[1,5] The role of CYTOP is similar to that of PαMS reported by Baeg *et al*.[5] Indeed, electrons injection from Al/C60 would be charged/discharged by the CYTOP layer, causing conductivity modulations of the C60 channel of the transistors. The gate currents (I_G) of the transistors are presented in Fig. 2(c). The I_G obtained during the transfer characterizations of programmed and erased states were almost similar to that of initial I_G, meaning negligible leakage of electron storage.

Figure 3(a) exhibits the shifts in V_{Th} and μ as a function of program voltage. For program, the V_{Th} rose up at a certain voltage of 40 V and significantly at a voltage of 50 V. Meanwhile, for erase, the V_{Th} gradually decreased with increasing negative voltages and reached to the initial value at a voltage of -45 V. The μ almost did not change in all cases. The P/E voltages were chosen to be 50/-45 V. These values are ~50 V lower than that of previous reports.[5,6]

Endurance property of the memory transistor is shown in Fig. 3(b). The devices were well rewritable for several tens of cycles. To determine the nonvolatile memory properties of the devices, the drain current (I_D) of programmed and erased states were observed (Fig. 3(c)). Under both states, the I_D was continously measured at a drain voltage (V_D) of 4 V and at a V_G of 5 V. Significantly, the obtained I_D slightly changed after 10^5 s in both states, indicating high stability of stored data.

4. Conclusions

In summary, memory transistors with the chargeable polymer of CYTOP were successfully demontrated. The ΔV_{Th} of 10 V was obtained under proper program voltage. The conductivity of C60 channel of the transistor was controlled by electron storage in the CYTOP layer. The memory devices exhibited high stability of retention time characteristics. The constributions of current study are introduction a new chargable polymer of CYTOP and application in fullerene memory transistors.

References

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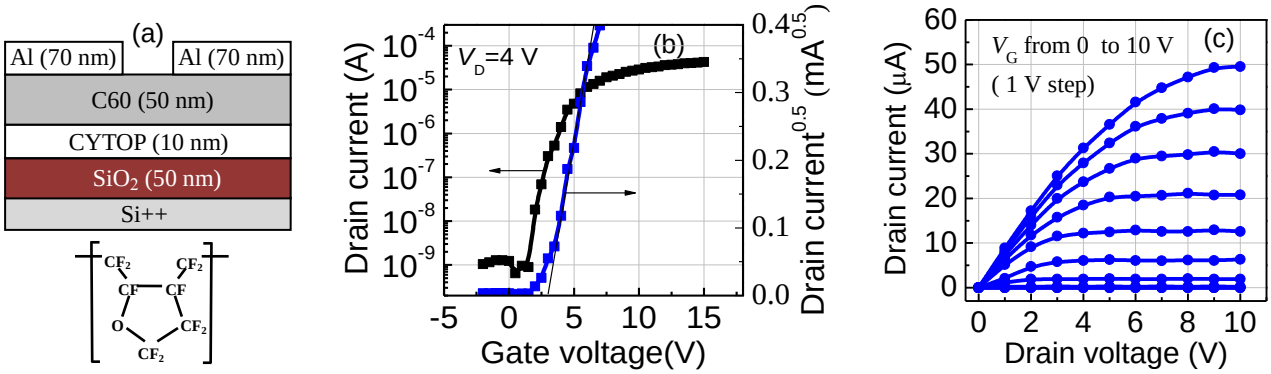

FIG. 1. (a) Schematic illustration of memory transistors and chemical structure of CYTOP. Transfer (I_D-V_G) (b) and output (c) characteristics of memory transistors. Transistors showed *n*-channel field-effect properties in the operation region of positive gate and drain voltages.

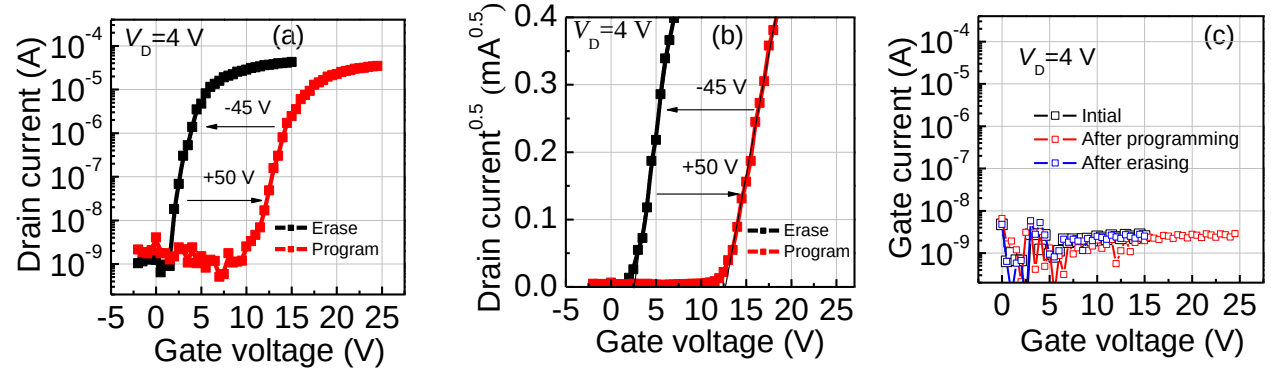

FIG. 2. I_D-V_G (a) and $(I_D)^{1/2}$-V_G (b) curves of memory transistor with respect to programming and erasing operations. Program and erase were done by applying gate pulse of 50 and -45 V for 100 ms while source-drain electrodes were grounded. Memory window was estimated to be 10 V. (c) Gate currents obtained during I_D-V_G characterizations of initial, programmed and erased states.

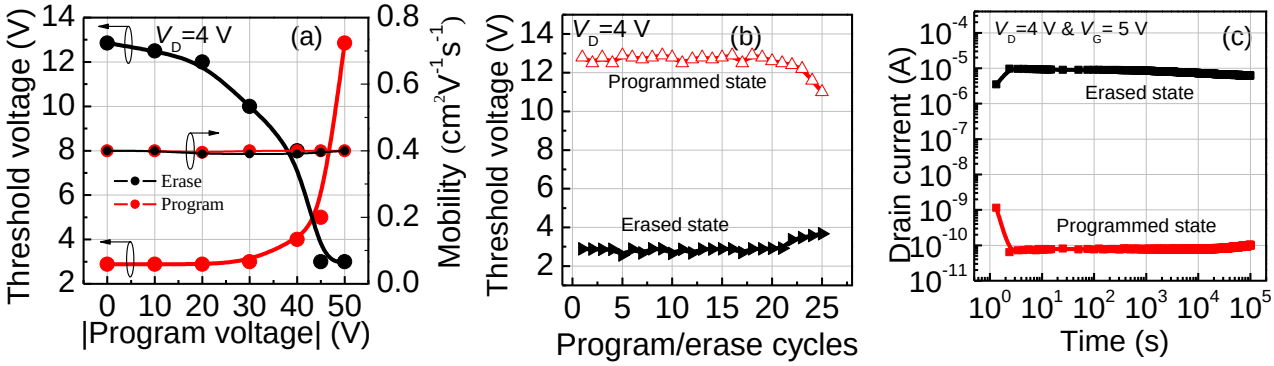

FIG. 3. (a) Changes in V_{Th} and μ of memory transistors as function of program voltage. Devices were programmed/erased by changing manitudes of gate pulses while source-drain electrodes were grounded. Width of each pulse was 100 ms. (b) Endurance characteristics of memory transistor with respect to number of program/erase cycles. Program and erase were carried out by applying gate pulse of 50 and -45 V for 100 ms while source-drain electrodes were grounded. (c) Retention time of I_D of programmed and erased states. I_D was continously measured at V_D of 4 V and at V_G of 5 V with zero source bias. On/off ratio remained ~0.8x10^5 after 10^5 s, suggesting high stability of states of memory transistors.