Scaling of the Pull-In Voltage in a Novel CMOS-compatible NEMS Switch

David J. Baek, Sung-Jin Choi, Dong-Il Moon, and Yang-Kyu Choi

Dept. of EE, KAIST, Daejeon 305-701, Korea
Phone: +82-42-350-3477, Fax: +82-42-350-8565, E-mail: ykchoi@ee.kaist.ac.kr

Abstract
A novel method for reducing the pull-in voltage and achieving a steep sub-threshold slope has been studied on a FinFET-based NEMS switch. By decreasing the gap between the gate electrode and the fin (beam) with a process compatible with the CMOS fabrication, the proposed device showed a pull-in voltage of 2 V and a sub-threshold slope of 5 mV/dec, which can be further improved. Along with this method, it is a viable candidate for future low-power electronic devices.

Introduction
Due to the physical limitation imposed by the finite sub-threshold slope of 60 mV/dec in FETs that work based on the diffusion transport mechanism, it is difficult to operate the transistors at low voltage with low leakage current. As a remedy to the above problem, many different alternatives have been suggested that either operate under different transport mechanisms [1] or present new switching device concepts [2]. Among the alternatives, NEMS switch has drawn great attention as the physical separation of the gate and channel allows for the standby leakage current to approach an infinitesimal number [3-4]. However, NEMS switch has its own drawbacks in that it requires a relatively high voltage for the pull-in operation. Although the pull-in voltage ($V_{p}$) itself can be lowered by shrinking the device dimensions, because the length and width of a beam affect the $V_{p}$ in a counter direction, scaling down the dimension alone cannot solve the problem. To investigate the above matters, in this paper, for a FinFET-based NEMS switch device that is fully compatible with the CMOS fabrication process [5], we present a novel method to reduce the $V_{p}$ without scaling the dimension and which only requires a simple step that can be added in the fabrication process.

Operating Principle and the Device Fabrication
As shown in the schematics in Fig. 1, the structure of this device is slightly modified from the double-gate FinFET by replacing the gate oxide with an air gap. The SEM and TEM images of the overall structure are illustrated in Fig. 2. The fabrication process of our device, explained in Fig. 3, is similar to that of a double-gate FinFET except for the removal of gate oxide [5]. The initial transfer characteristics of the double-gate FinFET before the gate oxide removal are shown in Fig. 4. By exposing the FinFET to a diluted HF solution, the gate oxide is removed and the channel (fin) region becomes suspended and movable. After completely etching the oxide layers, the exposed surfaces of the fin and the gates are re-oxidized according to three different conditions which lead to different oxide thicknesses as shown in Fig. 2(d). By delivering a voltage from either gate, the loose fin can move up and down to attach to the gate according to the mechanism illustrated in Fig. 5. As the fin attaches to the gate and closes out the air gap, the transformed state mimics the behavior of a conventional MOSFET as can be seen from the transfer characteristics in Fig. 6. In this work, the experimental results are attained from devices with a fin length of 1 μm and width ranging from 40 to 56 nm.

Scaling of the Pull-In Voltage
As with the other NEMS switch devices, the $V_{p}$ of our device can be reduced by modifying the dimensions such as the fin width ($W_{Fin}$) and gate length ($L_{G}$). From the Euler-Bernoulli beam equation, we can predict that as the $W_{Fin}$ decreases, the elastic constant decreases and results in reduced $V_{p}$ while the opposite case occurs for $L_{G}$. The results depicting the influence of varying $W_{Fin}$ and $L_{G}$ are illustrated in Fig. 7. For a conventional NEMS switch, it has been reported that there is a major trade-off between the $V_{p}$ and the pull-in delay ($t_{p}$). That is, higher switching speed requires smaller gaps which in turn require a stiffer beam. Unfortunately, dimension-wise, stiffer beam is actuated at higher $V_{p}$. Hence, merely scaling down the device dimension is hardly useful when two parameters counteract. Remarkably, without scaling the dimensions, we were able to adjust the thickness of the oxide layer during the re-oxidation step and lower the $V_{p}$ down to 2 V. Given that the gap between the gate and the fin is fixed, as we increase the oxide thickness ($T_{ox}$), the air gap decreases in turn. Therefore, as the dielectric constant of an oxide is greater than that of an air, the overall electric field between the gate and the fin increases and results in reduced $V_{p}$. The impact of $T_{ox}$ on the $V_{p}$ is shown in Fig. 8 and 9. Notably, as the $V_{p}$ was reduced, the sub-threshold slope became steeper with less off-current. Even when the fin is detached from the gates, though small, there is still an obvious electric field between the gate and the channel. Therefore, before the pull-in operation, as the fin approaches near the gate, a channel is formed and allows for the drain current to flow. Thus, the pull-in should occur at the lowest voltage possible to avoid large off-currents. As illustrated in Fig. 6, by increasing the $T_{ox}$ by only 3 nm, we were able to achieve a $V_{p}$ of 2 V and a sub-threshold slope below 5 mV/dec. As shown in Fig. 10, due to stiction, releasing the fin after it adheses to a gate requires a much higher voltage and therefore further study is necessary for reducing the voltage.

Conclusion
A novel method for reducing the $V_{p}$ was conducted on a FinFET-based NEMS switch. In this method, scaling down the device dimension is not necessary and it only requires the addition of a simple procedure during the conventional CMOS fabrication process. Thus, it offers further reduction of the $V_{p}$ after the dimension has been optimized.

References

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VT Implantation

S/D Activation

S/D Implantation

Poly-Si CMP

SiN Deposition

Process flow used to fabricate the Fig. 3

re-oxidation are performed to obtain three

NEMS switch. Three different conditions for

pull-in operation, the fin is attached to

ID

typical transfer characteristic of a MOSFET is

observed.

Fig. 4 Measured $I_D - V_{G1}$ characteristics of a
double-gate FinFET with different bias applied to

G2. As $V_{G2}$ either helps or disturbs the formation

of a channel, the above transfer characteristics

can be obtained.

Fig. 5 Operating principle. (a) With voltage

applied to $G1$, electrostatic force induces the

fin to pull-in towards $G1$. (b) Voltage applied
to $G2$ along with the elastic force (fin) cause

the fin to release from $G1$ and attach to $G2$.

Fig. 6 $I_D - V_{G1}$ characteristics of the NEMS

switch before and after the pull-in. After the

pull-in operation, the fin is attached to $G1$ and

a typical transfer characteristic of a MOSFET is

observed.

Fig. 7 Measurement of the relationship between the device scaling and the pull-in condition

for two different parameters, $W_{Fin}$ and $L_G$. (a) As the $W_{Fin}$ decreases, $V_{PI}$ is decreased. At the same $T_{Ox}$ smaller $W_{Fin}$ can also reduce the leakage current. (b) For a smaller $L_G$, $V_{PI}$ is larger. At the same $T_{Ox}$, smaller $L_G$ results in increased leakage current. Thus, $L_G$ and $W_{Fin}$ have opposite effect from each other.

Fig. 8 Change in $V_{PI}$ for different $T_{Ox}$. As $T_{Ox}$

increases, $V_{PI}$ is decreased. Again, for lower

$V_{PI}$, the leakage current is smaller. When $T_{Ox}$
is doubled, $V_{PI}$ decreases by more than a factor of four.

Fig. 9 Statistical results of the $V_{PI}$ against $W_{Fin}$

and $T_{Ox}$ at the same $L_G$. Although $V_{PI}$ is affected

by both $T_{Ox}$ and $W_{Fin}$, change in $T_{Ox}$, i.e.,

reduction of air gap, has a more drastic impact

on the pull-in condition.

Fig. 10 Pull-in and release operation. Blue is

the initial pull-in towards $G1$ while red is the

release from $G1$ and a subsequent pull-in

towards $G2$. Due to stiction from van der Waals force, $V_{PI}$ is much higher for red.