P-12-12

Extended Abstracts of the 2011 International Conference on Solid State Devices and Materials, Nagoya, 2011, pp454-455

High-Speed-Search Nonvolatile TCAM Using MTJ Devices

Shoun Matsunaga[1], Akira Katsumata[2], Masanori Natsui[1,2], Tetsuo Endoh[1,3], Hideo Ohno[1,4], and Takahiro Hanyu[1,2]

[1] Center for Spintronics Integrated Systems (CSIS), Tohoku University, JAPAN
[2] Laboratory for Brainware Systems, Tohoku University, JAPAN
[3] Center for Interdisciplinary Research, Tohoku University, JAPAN
[4] Laboratory for Nanoelectronics and Spintronics, Tohoku University, JAPAN
Phone: +81-22-217-5508, E-mail: {zhao-yun, katumata, natsui, hanyu}@ngc.riec.tohoku.ac.jp

1. Introduction

Ternary content-addressable memory (TCAM) is an attractive hardware engine with its high-speed fully-parallel data search. It is useful in a number of applications such as IP filters, network switches, look-up tables, and virus checkers [1, 2]. However, the TCAM consisting of volatile CMOS-based 16T (or 12T) cell circuit [3] has two major issues. First one is its increasing standby power due to leakage current in nanometer-scaled CMOS era. The other is its high bit-cell cost, because the TCAM cell needs two bit storage elements and a comparison logic element.

For realizing a standby-power-free and compact TCAM, we have proposed a nonvolatile magnetic-tunnel-junction (MTJ)-based TCAM with 6T-2MTJ-based cell using nonvolatile logic-in-memory circuit technique [4]. The chip area of the 6T-2MTJ-based nonvolatile TCAM can be certainly reduced, while the voltage swings of the cell circuit and match-line in a word circuit are limited because of weak driving capability of the cell circuit, which makes the match-line switching speed slowdown. In order to enjoy the benefit of the nonvolatile fully parallel TCAM, it is also an important issue to enhance search speed of the TCAM.

In this paper, we propose a 9T-2MTJ-based nonvolatile TCAM cell circuit where a compact single-end sense amplifier is embedded into each cell. The embedded amplifier enables to generate full swing voltage of each cell output for high-speed match-line switching capability. The transistor counts of the proposed cell is slightly larger than the previous 6T-2MTJ-based cell, but still smaller than the conventional CMOS-based volatile TCAM cells [3] or other MTJ-based nonvolatile TCAM cells [5].

2. MTJ-Based Nonvolatile Fully Parallel TCAM

Fig. 1 shows a structure and a symbol of a newly-developed perpendicular MTJ device, which uses large perpendicular magnetic anisotropy at the interface between an insulator and magnetic electrode [6]. The most important advantage of the perpendicular MTJ device over conventional in-plane MTJ device is its lower write current under high thermal stability. According to the spin direction of the free layer with respect to that of the fixed layer, there are two distinct states as the different resistances of the MTJ device; low resistance R_P when the spin directions are parallel and high resistance R_{AP} when anti-parallel. Thus, the MTJ device can be considered as a variable resistor, which indicates that the MTJ device has not only nonvolatile storage capability but also pseudo switching capability to build a logic device in accordance with stored data.

Fig. 2 shows an overall structure of a nonvolatile fully parallel TCAM. The TCAM is constructed by word circuits each of which consists of a nonvolatile TCAM cell array with a sense amplifier, decoders, and input/output drivers. In the nonvolatile fully parallel TCAM, the input signals in all bits of the search key are simultaneously applied to two-dimensional cell array, and equality-search operations in all word circuits are simultaneously performed. Thus, bit-parallel/word-parallel (fully parallel) equality search of the TCAM enables to realize high-speed data search. In addition, power dissipation, especially standby power dissipation due to increasing leakage current in nanometer-scaled CMOS era is one of the crucial issues. Therefore, a nonvolatile fully parallel TCAM is an attractive hardware in terms of standby-power-free TCAM.

Fig. 3 shows TCAM cell circuits with their truth table. Since TCAM has a masked equality-search function, each cell circuit has two bits of storage elements to store three kinds of data “0”, “1”, and “X” (don’t care). These data are encoded to 2-bit binary numbers (b_1, b_2) as shown in Fig. 3(a). CMOS-based TCAM cell consists of two SRAM cells (4T static storage elements in case of 12T-TCAM cell) and a comparison logic circuit as shown in Fig. 3(b). Fig. 3(c) shows the 6T-2MTJ-based cell circuit we previously reported [4]. In this cell, logic function and nonvolatile storage function are compactly merged into 2T-2MTJ comparison logic circuit part with peripheral circuit parts such as write transistors, a current-source-based load, and a diode switch. Since the limited voltage swing of the cell output is directly conducted to match-line through the diode switch, the match-line voltage swing which must be detected by sense amplifier is also limited to less than 1/3 of V_{DD}. Fig. 3(d) shows the proposed 9T-2MTJ-based cell circuit. Since a single-end compact sense amplifier is inserted into the cell circuit to generate full swing output voltage, the driving capability of the pass transistor connected between match-line and ground-line is greatly enhanced with short critical path (one transistor), which results in high-speed match-line switching.

Fig. 4(a) shows a simple design example of a nonvolatile fully parallel TCAM word circuit based on dynamic logic. Fig. 4(b) shows the simulated waveforms of the word circuit. In the precharge phase (CLK=Low), the match-line is precharged to V_{DD}. In the evaluate phase (CLK=High), the matched result is detected by the match-line voltage level. In case of “Match”, the match-line voltage is maintained to V_{DD}, because each pass transistor in the linear cell array is turned off. In case of “Mismatch”, the match-line voltage becomes 0 V, because one or more pass transistors in the linear cell array are turned on. During detecting the “Mismatch”, full voltage V_{DD} is applied to each pass transistor in the mismatched cells, which enables to enhance the discharge speed of match-line.

Fig. 5 summarizes the comparison results of the 144-bit word circuits between 6T-2MTJ-cell type, the proposed 9T-2MTJ-cell type, and 12T-CMOS-cell type. The attractive feature of both 6T-2MTJ-cell type and 9T-2MTJ-cell type is nonvolatility which can eliminate standby power. Since the proposed 9T-2MTJ cell has not only high driving capability by full swing output voltage but also short critical path between match-line and ground-line in exchange for the slight increase of area cost, delay of the 9T-2MTJ-cell-based word circuit is reduced to about 40 % compared with other two types. Note that estimated area cost of the proposed cell is less than or equal to that of conventional CMOS-based cell. As the result, search speed of the 9T-2MTJ-cell-based word circuit is enhanced to about 250 %.

3. Conclusions

In this paper, we have proposed a 9T-2MTJ-based cell circuit toward a high-speed and standby-power-free TCAM. The proposed TCAM cell effectively achieved the search speed with full-voltage-swing cell operation compared to previous 6T-2MTJ-based nonvolatile TCAM and 12T-CMOS-based volatile TCAM. The proposed cell is realized with smaller transistor counts compared to the conventional CMOS-based cell, while having nonvolatility. As a future prospect, it is important to investigate the power management methods to effectively reduce the standby power in the nonvolatile TCAM.

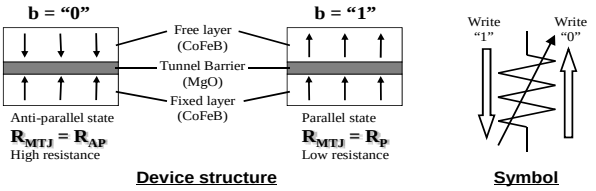

Fig. 1 Perpendicular MTJ device.

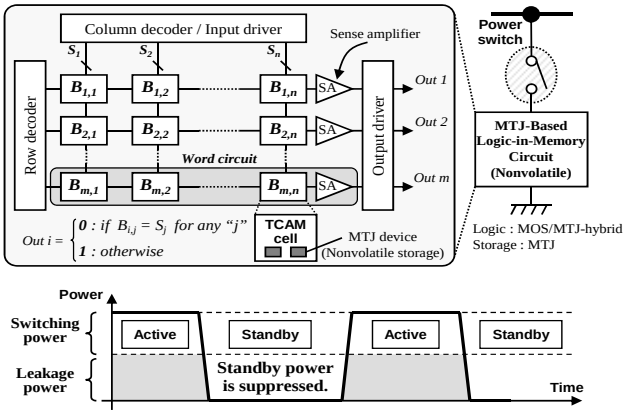

Fig. 2 Overall structure of a nonvolatile TCAM.

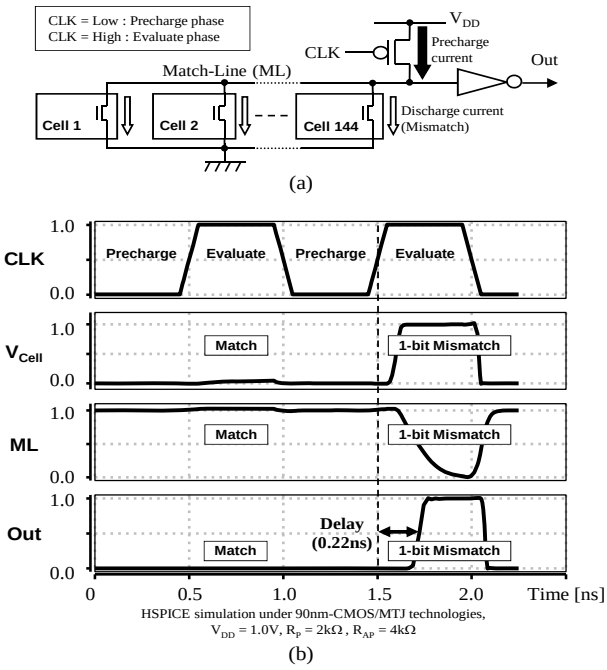

Fig. 4 9T-2MTJ-cell-based 144-bit TCAM word circuit : (a) design example of the word circuit, (b) simulated waveforms.

Acknowledgements

This research is conducted under "Research and Development of Ultra-Low Power Spintronics-based VLSIs" (Project leader: Hideo Ohno), which is supported by the Japan Society for the Promotion of Science (JSPS) through its "Funding Program for World-Leading Innovative R&D on Science and Technology (FIRST Program)." This research is also supported by VLSI Design and Education Center (VDEC), the University of Tokyo in collaboration with Synopsys, Inc.

References

[1] K. Pagiamtzis, et. al. : IEEE J. Solid-State Circuits **41** (2006) 712.
[2] C.-C. Wang, et. al. : IEEE J. Solid-State Circuits **44** (2009) 1571.
[3] I. Arsovski, et. al. : IEEE J. Solid-State Circuits **38** (2003) 155.
[4] S. Matsunaga, et. al., IEEE Int. Symp. Multiple-Valued Logic (2011) 99.
[5] Wei Xu, et. al. : IEEE Trans. VLSI Systems **18** (2010) 66.
[6] S. Ikeda, et. al. : Nat. Mater. **9** (2010) 721.

Stored data		S (Input data)	ML (Matched result)
B	(b_1,b_2)		
0	(0,1)	0	**High (Match)**
		1	**Low (Mismatch)**
1	(1,0)	0	**Low (Mismatch)**
		1	**High (Match)**
X (Don't care)	(0,0)	0	**High (Match)**
		1	**High (Match)**

(a)

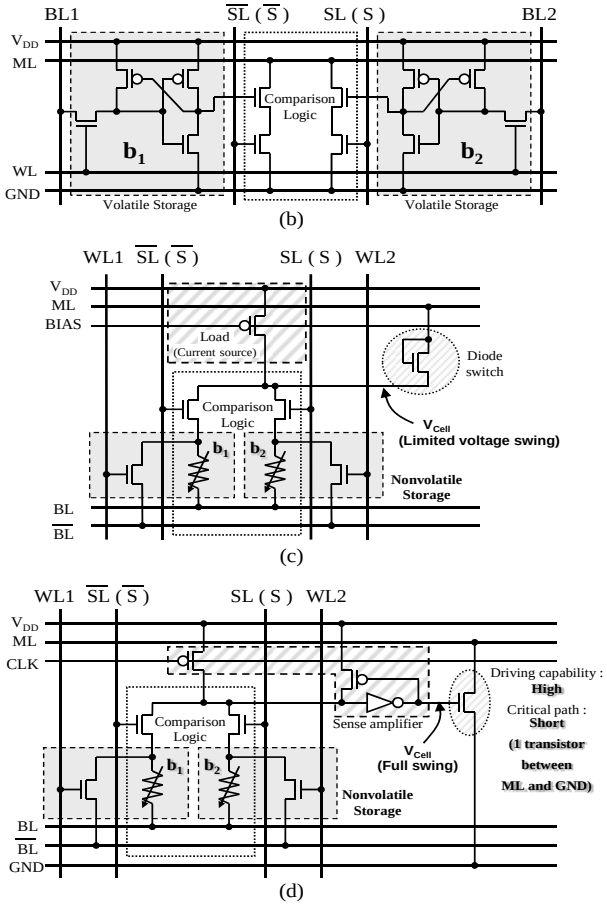

Fig. 3 TCAM cell circuits : (a) truth table, (b) 12T-CMOS-based, (c) 6T-2MTJ-based, (d) 9T-2MTJ-based.

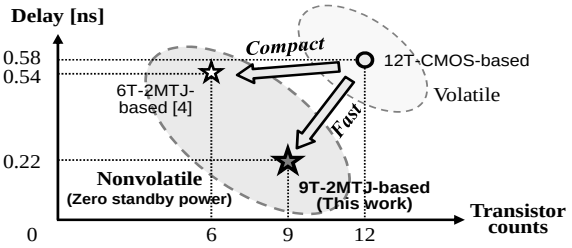

Fig. 5 Comparison results of 144-bit TCAM word circuits.