Extended Abstracts of the 2011 International Conference on Solid State Devices and Materials, Nagoya, 2011, pp486-487

Selective-area-grown graphene transistors by thermal chemical vapor deposition method

Makoto OKAI[1], Kumiko TOKUMOTO[2], Takashi KYOTANI[2],
Masahide TOKUDA[3], Ken TSUTSUI[3], and Yasuo WADA[3]

Hitachi Research Lab., Hitachi Ltd. [1],
7-1-1, Omika, Hitachi, Ibaraki 319-1292, Japan
Phone: +81 294 52 5111 (ext. 6591), E-mail: makoto.okai.ev@hitachi.com

Inst. of Multidisciplinary Research for Advanced Materials, Tohoku Univ.[2],
Bio-Nano Electronics Research Center, Toyo Univ. [3]

1. Introduction

Graphene is a single atomic layer of carbon atoms that form a honeycomb structure, and thus, it is the ultimate thin layer. Thanks to its high carrier mobility, graphene is one of the materials with most promise to open a new era of electrical and optical integrated circuits. A method needs to be developed to grow graphene directly on sub-nm-order flat insulating layers in order to fabricate electrical and optical devices that utilize graphene. In addition, using a Si wafer as a substrate is strongly desirable. The current big Si-electronics industry has accumulated enormous amounts of knowledge and know-how concerning Si. Thus, starting graphene-electronics on a Si substrate seems practical.

We recently reported on a growth method for graphene on a sapphire substrate [1] and on an Al_2O_3 layer sputter-deposited on a SiO_2/Si substrate [2]. This paper presents a new selective-area growth method for graphene on a fine-patterned Al_2O_3 layer fabricated on a SiO_2/Si substrate. We fabricated graphene transistors successfully utilizing this selective-area growth method and obtained their excellent electrical characteristics.

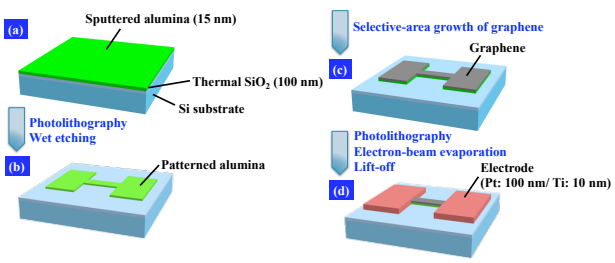

Fig. 1. Fabrication process for graphene transistor utilizing selective-area-grown graphene as channel.

2. Experimental procedure

Our fabrication process for graphene transistors is shown in Fig. 1 and as follows: A sputter-deposited Al_2O_3 layer (15 nm thick) on SiO_2 (100 nm thick)/Si substrate is patterned to channel, source, and drain regions. The source and drain regions are connected by the channel region. Graphene layers are grown on the patterned Al_2O_3 regions selectively with no growth on SiO_2 surface by thermal chemical vapor deposition method. The catalytic ability of Al_2O_3 for graphene

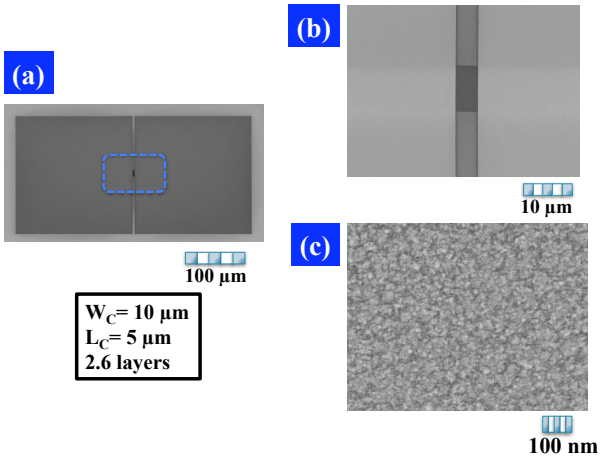

Fig. 2. Scanning electron microscope views of the fabricated graphene transistor. (a) Whole device. (b) Enlarged image of the area surrounded by broken line in (a). (c) Enlarged image of channel region.

growth is approximately ten times larger than that of SiO_2.The growth temperature is 800 ˚C and using propylene flows (4 ml/min) as the source gas and argon (400 ml/min) as the carrier gas. The graphene layers have piled structure of small platelets with a domain size of 30 nm. The averaged number of layers is 2.6 for 2-minute growth. The source and drain regions are covered with Au (100 nm thick)/Ti (10 nm thick) electrodes by using electron beam evaporation method and lift-off process.

3. Results and discussion

Scanning electron microscope views of the fabricated graphene transistor are shown in Fig. 2. The source and drain electrode are 150-μm square as shown in Fig. 2(a). We confirmed that graphene platelets piled on the channel region selectively as shown in Fig. 2(b) and (c). We also checked that there is no electrical conductivity on SiO_2 surface.

The electrical characteristics of the fabricated graphene transistor with a channel width (W_C) of 2 μm, a channel length (L_C) of 5 μm, and averaged number of graphene layers of 0.5 are shown in Fig. 3 and 4. The gate voltage is applied to the substrate. The drain current decreases as the gate voltage increases form -40 V to 0 V as shown in Fig. 3. The on/off ratio of the drain current is 20.6 when the drain voltage is 10 V and the gate voltage ranges from -40 V to +40 V as shown in Fig. 4. Forty-six devices among 50 give on/off ratio more than 10 and the yield of high on/off ratio is 92%.

We also fabricated graphene transistors with averaged number of graphene layers of 2.6. They give poor on/off ratio less than 2.

The graphene layer is not continuous when the averaged number of layers is less than one, and there is a chance that the channel width is partially as narrow as the domain size of 30 nm. We suppose that the narrow channel effect gives an effective band-gap that results in the high on/off ratio.

4. Conclusions

We fabricated graphene transistors utilizing selective-area-grown graphene as channel. A high on/off ratio more than 20 is achieved when averaged number of graphene layer is 0.5.

References

[1] M. Okai, et al., Tenth International Conference on the Science and Application of Nanotubes 2009 (Beijing, China), paper D13, 2009.

[2] M. Okai, et al., Carbon 2010 (Clemson, USA), paper Th-2A-5, 2010.

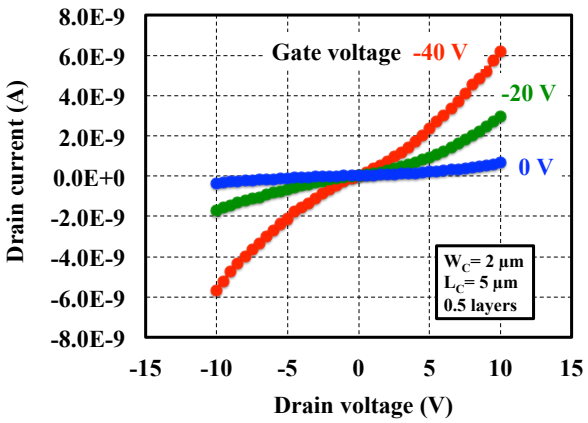

Fig. 3. Drain current as a function of drain voltage for various gate voltage.

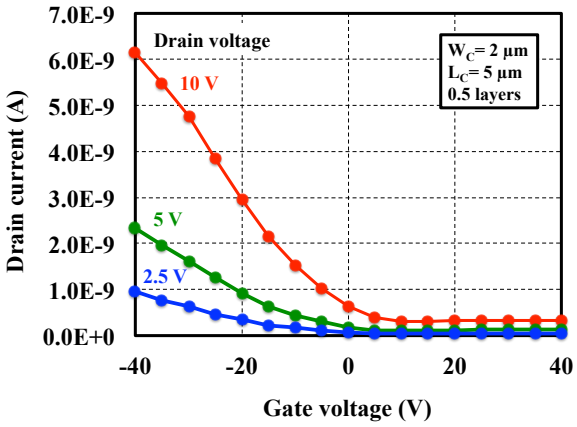

Fig. 4. Drain current as a function of gate voltage for various drain voltage.