Extended Abstracts of the 2011 International Conference on Solid State Devices and Materials, Nagoya, 2011, pp466-467

P-13-2

Analysis of Bottom Channel Effect in Silicon Nanowire FET based on Bulk-Silicon: Reduction of Parasitic Capacitance caused by SiGe layer

Myung-Dong Ko[1], Sang-Hyun Lee[1], Rock-Hyun Baek[1], Chan-Hoon Park[1], Chang-Woo Sohn[1], Chang-Ki Baek[1,3], Jeong-Soo Lee[1,2], Yoon-Ha Jeong[1,2]

[1]Dept. of Electrical Engineering, Pohang University of Technology and Science (POSTECH), Pohang, Korea
Phone: +82-54-279-2897 E-mail: mdko84@postech.ac.kr
[2]Division of IT Convergence Engineering, Pohang University of Technology and Science (POSTECH), Pohang, Korea
[3]National Center for Nanomaterials Technology (NCNT), Pohang, Korea

1. Introduction

The silicon nanowire FET (SNWFET) is considered to be the most desired candidates from the viewpoint of outstanding scalability, excellent gate controllability and short channel effect immunity [1], [2]. Most of SNWFETs are fabricated with top-down technology on Si-On-Insulator (SOI) wafers or bulk-Silicon wafers [1]-[3]. Although SNWFETs on SOI have benefits in electrical performance [4], many SNWFETs are fabricated on bulk-Silicon to reduce the production cost. In the process of SNWFETs on bulk-Silicon, the additional channel should be made inevitably in the bottom silicon. This bottom transistor may contribute the current enhancement, but its amount is normally smaller than that of the intrinsic nanowire channel. In the view point of capacitance characteristics, however, the bottom channel results in significant parasitics due to capacitance between gate and bulk.

In this paper, we analyze the effect of bottom channel on the current and capacitance characteristics in the SNWFET on bulk-Silicon and investigate how to reduce the parasitic capacitance using the numerical simulation.

2. Structure features of SNWFET and simulation method.

Figure 1 shows a schematic cross-section of SNWFET. Since the gate-all-around nanowire channel is putting up on the bulk Silicon, there are a channel surrounded by the gate and a channel forming on the surface of bottom silicon. The nanowire channel is made of intrinsic silicon with a diameter of 20nm and a circumference width of 64 nm. It is surrounded by the silicon dioxide with a thickness of 3.3 nm and the TiN gate. Donor concentration for the source/drain (S/D) region is 10^{20} cm^{-3} and the SiGe layer with thickness of 40 nm is placed between the S/D region and the bottom silicon. The essential features of the used device consist of growing Si/SiGe layer on bulk Silicon are reported in detail in [1].

For these SNWFETs, the current-voltage characteristics were measured using the semiconductor parameter analyzer and the capacitance-voltage characteristics were measured using the LCR meter with the grounded S/D terminal and the opened bulk terminal [2].

We also perform the numerical simulation by non-equilibrium green function (NEGF) approach with coupled mode space (CMS) method since it has been favored when considering quantum mechanics effects on ultra small devices [5].

3. Result and discussion for bottom channel effect

A. Bottom channel effect

Figure 2 shows the measured drain current (I_d) and gate capacitance (C_{gsd}) as a function of the gate bias. The current-voltage characteristics show high $I_{on/off}$ ratio (~10^7) and low subthreshold swing (~70 mV/dec) indicating excellent gate controllability. In the capacitance-voltage characteristics, however, abnormal kink is observed at V_G = 0.85 V regardless of the gate length. This is attributed to the turn-on effect of the bottom transistor. As shown in Fig. 1, the electron channel is formed through not only the nanowire but also the bottom silicon. The bottom transistor is turned on by the gate bias when the energy barrier of SiGe layer is low enough for electrons to surmount the energy barrier.

To investigate this effect more clearly, we carry out the numerical simulation as shown in Fig 3. In the current-voltage characteristics, the drain current of bottom transistor is much lower than that of nanowire transistor although the bottom channel is sufficiently formed. The total drain current is almost same as the nanowire drain current. On the contrary, the bottom channel capacitance appears remarkably at the capacitance-voltage characteristics. The gate capacitance C_{gsd} starts to increase near V_G = 0.4 V by turning on the nanowire transistor. After V_G = 0.85 V, the bottom transistor is also turned on and C_{gsd} becomes sum of the nanowire channel capacitance and the bottom channel capacitance. Since there is the energy difference of conduction band between the S/D region and the SiGe layer, electrons from S/D are blocked by the energy barrier and cannot be injected to the bottom silicon. As the gate bias sufficiently increases, the energy barrier of SiGe layer lowers and the bottom channel plays a role as a parasitic capacitance.

It is unavoidable to fabricate SNWFET on the bulk-Si in the cost effective way. To analyze C-V characteristics of intrinsic nanowire channel, it is required to reduce the parasitic capacitance of bottom channel.

B. Methods to reduce the parasitic capacitance

Basic concept of reducing the bottom capacitance is to shift the turn-on voltage of bottom transistor by prohibiting electrons from accumulating at the SiGe layer. First, we change the spacing between SiGe layer and gate electrode (T_S) which affects the gate controllability to electron accumulation at SiGe layer (Fig 4). It turns out that increasing T_S results in decreasing the gate controllability, thus it cause the increase in turn-on voltage of bottom transistor. The level of normalized total capacitance is also decreased with increasing T_S but it is attributed to decreasing overlap capacitances. As shown in Fig. 5, increasing T_S reduces the overlap capacitance (C_{ov}) among S/D region, SiGe layer and gate electrode, but it has nothing to do with the nanowire capacitance. Therefore, controlling the spacing between SiGe layer and gate electrode, i.e., gate trimming process is effective to reduce both bottom and overlap capacitances.

Another method of suppressing the bottom capacitance is enhancing the p-type doping concentration of SiGe layer. This method is effective when the gate trimming technique (increasing T_S) is not available. Since the turn-on voltage of

bottom transistor is determined by the point of populating electrons in SiGe layer, inducing acceptors to SiGe layer causes increasing the turn-on voltage. Figure 6 shows the normalized gate capacitance as a function of p-type (BF_2) doping concentration. As the doping concentration increases, the turn-on voltage increases (inset of Fig. 6) and the bottom capacitance becomes suppressed. As shown in Fig. 7, moreover, the drain current flowing through bottom channel is almost eliminated with high doping concentration in SiGe layer. Therefore, total current and capacitance at this situation is very close to those of SNWFET on SOI.

4. Conclusion

We have analyzed the effect of bottom channel on the current and capacitance characteristics in the SNWFET on bulk-Si. Although the bottom channel insignificantly contributes to the drain current, it causes parasitic capacitance and distorts the capacitance characteristics of intrinsic nanowire when gate bias is large enough to turn on the bottom transistor. To reduce bottom capacitance, we have proposed two methods, the gate trimming technique and the SiGe doping technique. These methods prohibit electrons from accumulating at the SiGe layer, thus increase the turn-on voltage of bottom transistor. With the SiGe doping technique, we cost-effectively fabricate SNWFET on bulk-Si instead of on SOI while anticipating the similar performance of SNWFET on SOI.

Acknowledgements

This research was supported by World Class University (WCU) program through the National Research Foundation of Korea funded by the Ministry of Education, Science and Technology (R31-2010-000-10100-0). This work was partially supported by the BK21 program and system IC 2010 program, the National Center for Nanomaterials Technology (NCNT) in Korea.

References

[1] S. D. Suk *et al.*, IEDM Tech. Dig., pp. 717, 2005
[2] R. H. Baek *et al.*, IEEE EDL, vol. 32, pp. 116, 2011
[3] D. W. Kim *et al.*, IEEE SOI Conf., pp.117, 2008
[4] J. Zhuge *et al.*, IEEE TED, vol. 9, pp. 114, 2010
[5] M. Luisier *et al.*, J. Appl. Phys., vol. 100, pp.043713, 2006

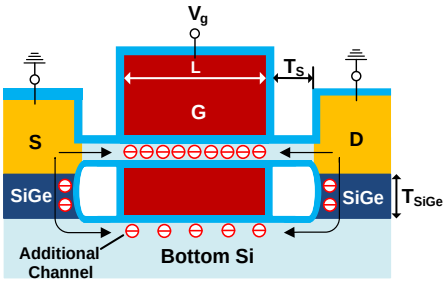

Fig. 1. The schematic cross-section of SNWFET. In the SNWFET on bulk Silicon, additional channel should be made unavoidably, which has to be considered in the view of operation.

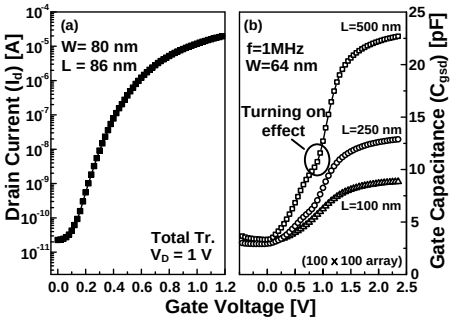

Fig. 2. (a) Measured total drain current (I_d) from SNWFET at V_D = 1 V. (b) Measured total C_{gsd} from SNWFET at 1MHz. At V_G = 0.85 V, turn-on effect is appeared.

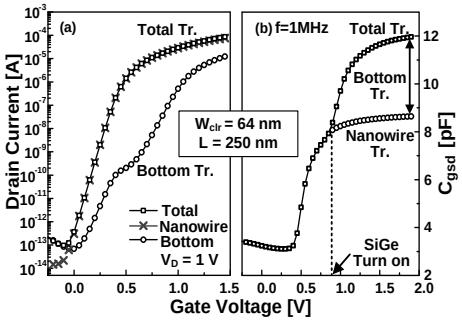

Fig. 3. The simulated drain current and capacitance data at W_{clr} = 64 nm and L_G = 250 nm. Bottom channel capacitance is generated after turn-on voltage.

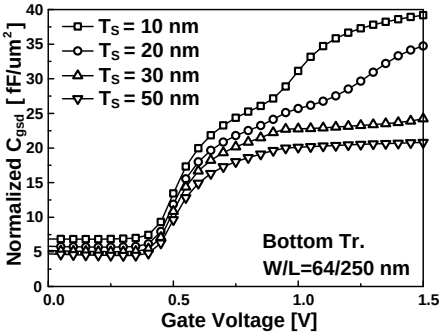

Fig. 4. Normalized C_{gsd} with different distance between SiGe layer and gate. Bottom capacitance is diminished with increasing T_S.

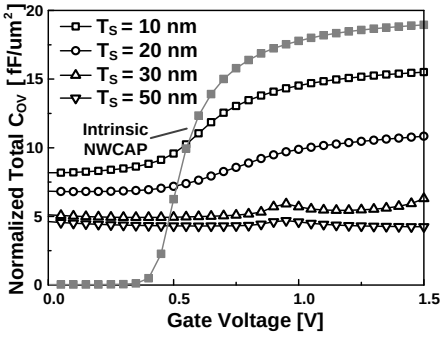

Fig. 5. Total normalized C_{ov} and intrinsic nanowire capacitance only. Over the T_S = 30 nm, C_{ov} is almost same.

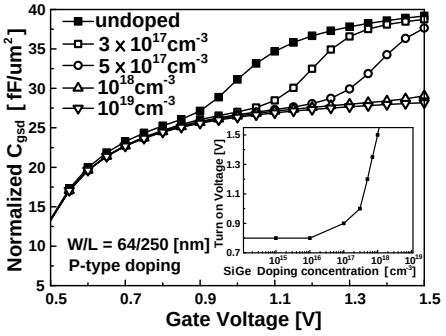

Fig. 6. Normalized C_{gsd} with different p-type (BF_2) doping concentration of SiGe layer. The turn-on voltage is increased and C_{gsd} is shifted to positive direction.

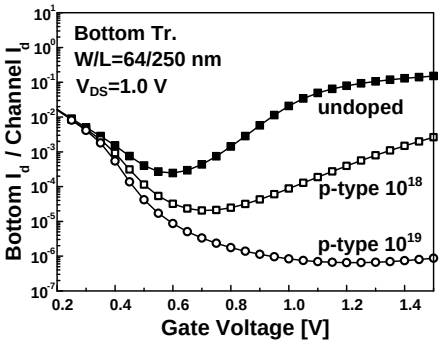

Fig. 7. The proportion of bottom current and channel current according to p-type (BF_2) concentration. In the high doping concentration, bottom current is almost eliminated.