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Interfaces of High-k Gate Insulator in Carbon Nanotube FETs

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1. Introduction

Carbon nanotubes are one of promising materials for CMOS devices because of their high carrier mobility for both of electrons and holes. For CMOS applications, it is necessary to control the polarity of conduction carriers. In the previous study, we have realized air-stable, high-performance, Si-process compatible, n-type carbon nanotube field-effect transistors (CNFETs) and CMOS inverters, utilizing fixed charges in the high-k gate insulator deposited by atomic layer deposition (ALD) [1, 2]. However, we have not fully understood the location and origin of the fixed charges, nor their effect on the device property.

In this study, we have studied the electrostatic property of the interfaces of the gate insulator layer by Kelvin probe force microscopy (KFM). Charge distributions are measured for the interfaces between HfO_2 and a Au contact and between HfO_2 and a SiO_2/Si substrate. In addition, the formation of interface dipole is investigated for a-few-monolayer HfO_2 layer.

2. Experimental

Figure 1(a) and (b) show the schematic structures of the samples used in this study to measure the interface charges by KFM. These structures respectively imitate the gate insulator on the source (drain) contact electrodes, and the gate insulator on the SiO_2/Si substrate in CNFETs. The HfO_2 was deposited on a Au electrode or on a 10-nm-thick-SiO_2/Si substrate by ALD technique at 250˚C, followed by post-deposition annealing at 300˚C in vacuum. Then, the HfO_2 layer was partially removed by reactive ion etching.

The circuit configuration for KFM measurement is also schematically shown in Fig. 1. In the KFM measurement, V_{DC} is adjusted so that the electrostatic force between the tip and sample becomes zero, thus the contact potential difference (V_{CPD}) is measured as $-V_{DC}$. The V_{CPD} was measured at room temperature in vacuum with a Au-coated conductive tip.

3. Results and discussion

First, we studied the interface between the contact electrode and the gate insulator with the sample shown in Fig. 1(a). Figure 2 shows the line profile of V_{CPD} measured by KFM for the thickness of HfO_2 of 6 nm. The surface potential of the HfO_2 layer (V_s), which is given by the difference between V_{CPD}'s measured on the HfO_2 surface and on the Au surface, was about 0.9 V. The surface potential of HfO_2 increased with the thickness of the HfO_2 layer (t), and saturated at about 10 nm as shown in Fig. 3. The maximum surface potential was about 1 V. The space charge ($N(t)$) in the HfO_2 layer was evaluated from the thickness dependence by

$$N(t) = \frac{\varepsilon_0 \varepsilon_r}{qt} \frac{\Delta V_s}{\Delta t}, \qquad (1)$$

where $\varepsilon_0\varepsilon_r$ is the dielectric constant and q is elementary charge. Figure 4 shows the space charge distribution in the HfO_2 layer. This result indicates that most of the positive charges distribute within 10 nm from the interface. The integrated sheet charge density was 4.5×10^{13} cm^{-2}.

We also studied the interface between the HfO_2 gate insulator and a SiO_2/Si substrate. Figure 5 and 6 shows the surface potential of the HfO_2 layer on the SiO_2/Si substrate, and the space charge distribution in the HfO_2 layer, respectively. The integrated sheet charge density was 6.1×10^{13} cm^{-2}. In addition, we found that a one-monolayer deposition of HfO_2 built up the surface potential by $\Delta \sim 0.4$ V. This suggests an existence of the interface dipole layer between the SiO_2 and HfO_2.

Figure 7 summarizes the schematic energy diagrams suggested from this study for (a) the HfO_2/Au structure and (b) the HfO_2/SiO_2/Si structure. The positive charges distributing near the interface build up the potential in the HfO_2 layer. In the case of HfO_2/SiO_2 interface, the potential varies abruptly at the interface due to the interface dipole.

4. Conclusions

We have studied the interfaces of HfO_2 gate insulator for CNFETs by KFM. The results show the positive charges distribute near the interfaces between the HfO_2 and Au contact and between the HfO_2 and the SiO_2/Si substrate. In addition, it was suggested that there existed an interface dipole between the HfO_2 and SiO_2/Si substrate.

Acknowledgements

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References
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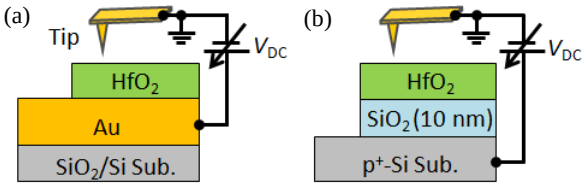

Fig. 1 Schematics of samples measured by KFM for (a) the interface between HfO_2 and Au and (b) the interface between HfO_2 and SiO_2/Si substrate.

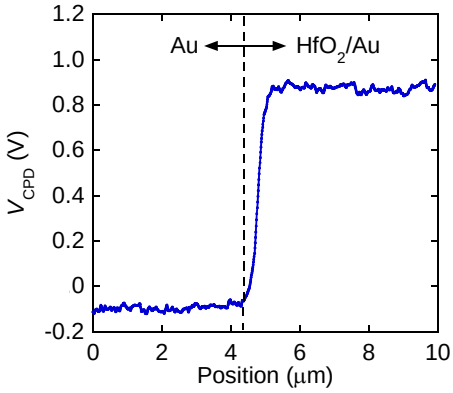

Fig. 2 Line profile of the V_{CPD} measured by KFM for the thickness of HfO_2 of 6 nm.

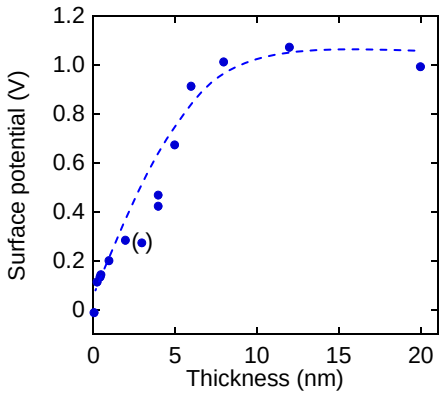

Fig. 3 Thickness dependence of the surface potential of HfO_2 layer on Au contact.

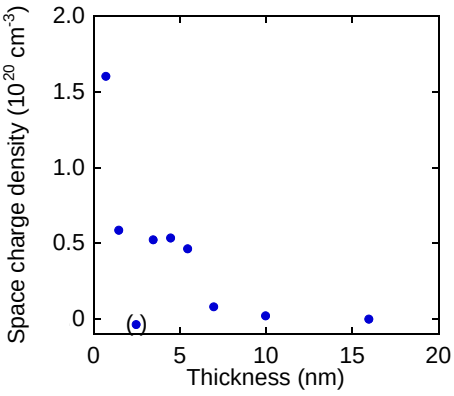

Fig. 4 Charge distribution in HfO_2 layer on Au contact evaluated from the thickness dependence of the surface potential.

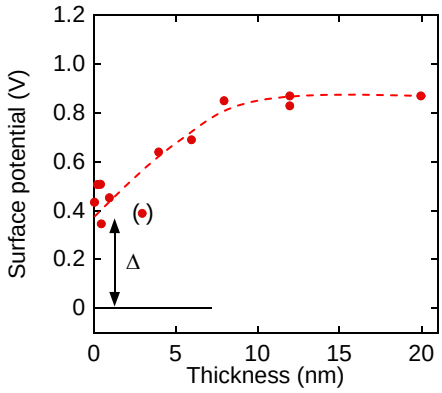

Fig. 5 Thickness dependence of surface potential of HfO_2 layer on SiO_2/Si Substrate.

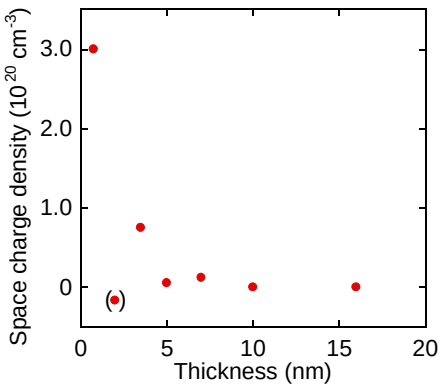

Fig. 6 Charge distribution in HfO_2 layer on SiO_2/Si substrate

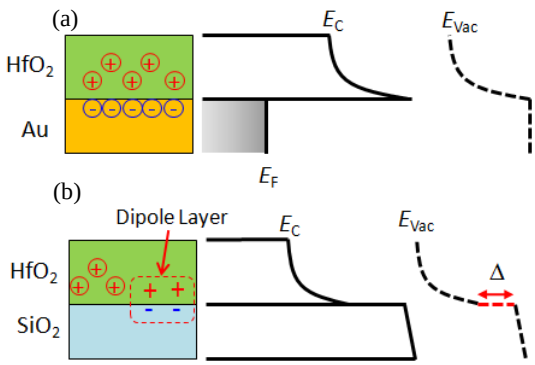

Fig. 7 Schematic energy diagrams of (a) the HfO_2/Au structure and (b) the HfO_2/SiO_2/Si structure.