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# A Multi Switching Current Study of Single-Electron Transistors Using Side Gate Bias Effect

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## 1. Introduction

Recently, single-electron tunneling phenomena in silicon nanostructures have been widely researched in terms of multifunctional logic and ultra-low-power nanoelectronic device applications. In comparison with heterostructures,[1] the possibility and application of the integration of the silicon nano structure into complementary metal-oxide-semiconductor (CMOS) devices have special advantages. Until now, various single-electron tunneling devices have been fabricated with silicon-on-insulator (SOI) nanowires. Various novel approaches have been used to increase operation temperature. Furthermore, room-temperature single-electron circuits have been demonstrated.

In this study, a room-temperature operating SET based on an electrically formed quantum dot is fabricated by conventional CMOS processes such as polycrystalline silicon (poly-Si) sidewall formation on the recessed channel structure. The Coulomb island on the channel is formed by a poly-Si sidewall gate with electrical tunneling barriers. Also, by using the side gate bias of the device, the drain current and oscillation peaks are effectively modulated.

## 2. Device Structure and Fabrication Process

Figure 1 shows a schematic of the fabricated device. The quantum dot (QD) is caused by the electrically induced tunneling barriers on the active surface. The device has a recessed structure and poly-Si sidewall gates on the channel, as shown in Fig. 1. In Fig. 1, the voltage, $V_{CG}$, of the n-doped poly-Si control gate modulates the potential of the Coulomb island, which is defined by two tunneling barriers induced by the side-gate bias $V_{SG}$. The top silicon layer with a boron doping concentration of $1 \times 10^{15}$ cm$^{-3}$ is thinned to 100 nm through a series of thermal oxidation and silicon oxide wet-etch steps. The active region is defined using electron-beam/photo mix-and-match lithography and a subsequent silicon plasma etching process, as shown in Fig. 2(a). 2(a) shows a schematic three-dimensional (3D) layout of the completed channel and source/drain structure. Figure 2(b)~(f) show schematics of the process sequence for forming a recessed channel, side gate, and control gate pattering method. First of all, an oxide layer is deposited about 200 nm by a low pressure chemical vapor deposition (LPCVD) on the active surface, as shown in Fig. 2(b). Subsequently, the poly-Si layer of 40 nm is deposited on the oxide layer. The poly-Si layer is pattered by an electron-beam (E-beam) lithography using a styrene methyl acrylate-based positive electron beam resist (ZEP 520A) mask and subsequent plasma silicon etch and oxide etch process, as shown in Fig. 2(c). Next, the silicon nanowire at the patterned region is partially etched in Fig. 2(d). For further narrowing the quantum dot size and curing plasma etch damage of channel, 10 nm of thermal oxide is grown on the channel region. Also, the grown oxide layer works as gate dielectric material. Then, to form two poly-Si sidewall spacers of 20 nm, $n^+$ doped poly-Si layer is deposited and etch-back is processed. These sidewall spacers work as side-gate, as depicted in Fig 2(e). Next, to form an inter-gate oxide, 10 nm of oxide is grown, as shown in Fig. 2(e). Afterward, 200 nm of a poly-Si layer for forming the control gate is deposited using the LPCVD process. In order to align the side gate and source/drain, poly-Si layer is planarized by etch back process, as shown in Fig. 2(f). Figure 3 shows the cross-sectional SEM images of a test wafer for Si nanowire, as shown in Fig. 3(a), the recessed channel structure of device as depicted in Fig. 3(b), and the control gate formation as shown in Fig. 3(c).

## 3. Results and Discussion

The process sequence of the fabricated device is highly compatible to that of the conventional CMOS. Figure 4 shows the ATLAS simulation result for the recessed channel structure. When the control gate bias is increased, the tunneling barrier height of the previously reported device is lowered together with the quantum dot potential in the previous case, as shown in Fig. 4(c). To fix the potential of the quantum dots independently, the side gate bias is constantly and simultaneously increased with the occurrence of the control gate bias in a recessed channel structure, which reduces electrical tunneling barrier lowering phenomena of the device.

The devices are characterized using a precision semiconductor parameter analyzer (HP 4155A). The transfer characteristic is obtained at room temperature as a function of the control-gate voltage $V_{CG}$ and the source/drain voltage $V_{DS}$, as shown in Fig. 5 shows the $I_{DS} - V_{CG}$ curve as a function of $V_{SG}$ with a channel width of 15 nm and a recessed channel length of 200 nm. The position of the drain current is well modulated by $V_{SG}$. In the measurement results, the gradual decrease in drain current with side gate bias variation is attributed to the increases in the height and length of electrical potential barriers caused by the negative larger $V_{SG}$, as shown in Fig. 5(c). In addition, from the $I_{DS} - V_{CG}$ curve characteristic, it can be noted that the drain current is decreased when the side gate bias is increased by a negatively larger $V_{SG}$ with steps of 0.002 V. No drain current peaks can be observed even at the side gate bias from 0.44 to 0.3 V with steps of 0.002 V.

In Fig. 9, room temperature transfer characteristics of

fabricated devices with different side gate biases are shown. The transfer characteristics of the side gate bias are from 0.5, 0.434, and 0.3 V to 0.15, 0.276, and 0.142 V with steps of 0.005, 0.002, and 0.002 V, respectively. According to the rises and falls of an approved bias and changing the step of the side gate biases, the drain current and current slope of the fabricated device are modulated more effectually. It can be concluded that the drain current is controlled by the electrically induced tunneling barriers through the bias modulation on the side gates.

## 4. Conclusion

For practical device application, we have fabricated a DG-SET having a recessed channel and a side gate. The demonstrated device is much more compatible to conventional CMOS processes. Its transfer characteristics are obtained at room temperature. From the drain current, the current level and slope are clearly controlled by electrically formed potential barriers using the side gate bias in the same device at room temperature. This principle applies to multibit functionality for the practical implementation of the SET-based multivalued memory and logic device.

## 5. References


1) C. Thelander, T. Martensson, M. T. Bjork, B. J. Ohlsson, M. W. Larsson, L. R. Wallenberg, and L. Samuelson: Appl. Phys. Lett. **83** (2003) 10.


## Acknowledgements


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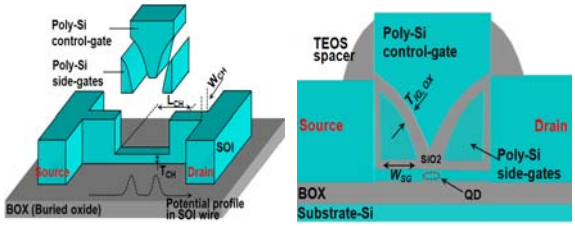
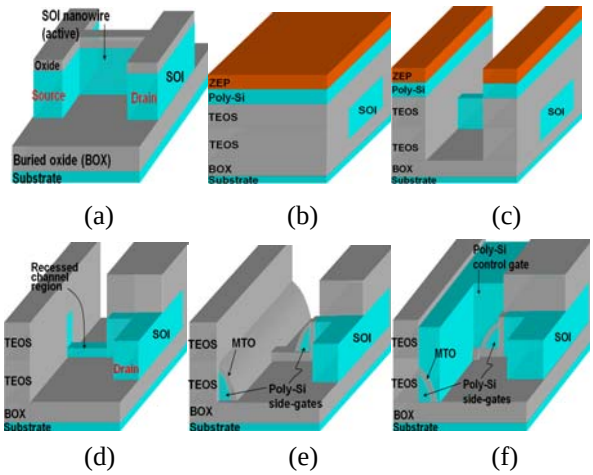



(a) (b)

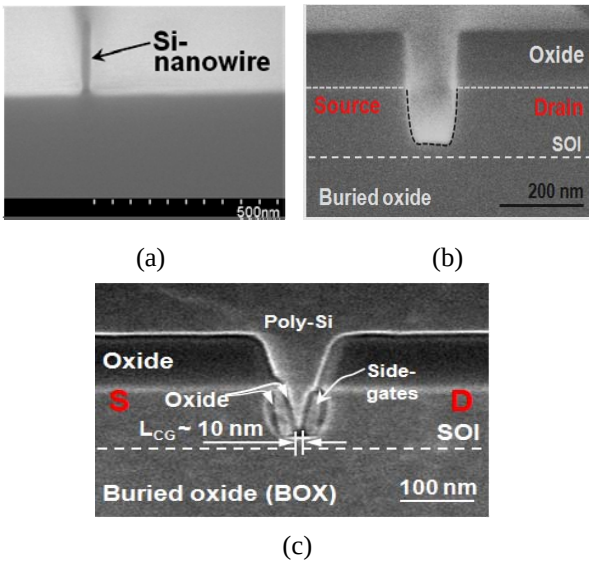
**Fig. 1.** Schematic three-dimensional layout of the proposed device having recessed channel structure (a) and oxide sidewall spacers around the control gate and potential profile along the channel by side gate bias (b).




(a) (b) (c)

(d) (e) (f)

**Fig. 2.** Schematics of the process sequence of the nanowire patterning methods using the mix-and-match and proposed fabrication process flows of the sidewall patterning process.




(a) (b)

(c)

**Fig. 3.** (a) Cross-sectional SEM images of a test wafer for Si nanowire, (b) recessed channel structure of device, and (c) control gate formation.

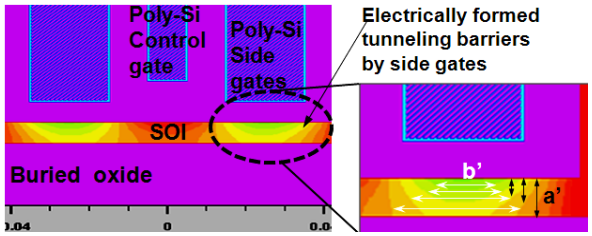



**Fig. 4.** Cross-sectional view along the channel region of the proposed device. Electrically potential distribution of the side gate bias when side gates are increased from 0.1 to 0.5 V.

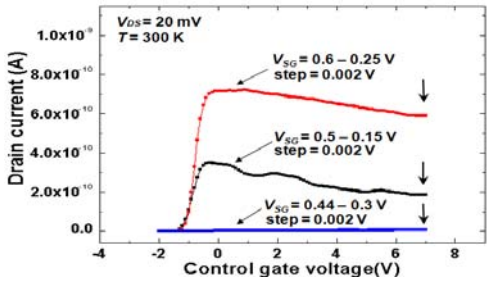



**Fig. 5.** Transfer characteristics of the fabricated device at room temperature. The drain current of the fabricated device is decreased when the control gate is increased.

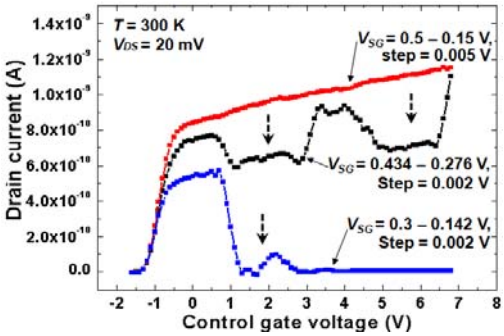



**Fig. 6.** Transfer characteristics of the fabricated SET with recessed channel structure with different side gate biases and bias steps in the same device at room temperature.