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Growth of GaAs Nanowires on Poly-Si by Selective-Area MOVPE

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1. Introduction

Semiconductor nanowires (NWs) have small diameters on the nanometer scales, and they are expected to fabricate high-efficient light-emitting diodes (LED) because of their high-aspect ratio and large surface area structures. We have fabricated III-V compound semiconductor NWs by using selective-area metalorganic vapor-phase epitaxy (SA-MOVPE). Using this method, the NWs have been formed on lattice mismatched substrates such as GaAs/Si [1] and InAs/Si [2] because of the limited area for crystal growth in the small openings of amorphous masks. Therefore, in this method, there is a lot of flexibility to select materials as a growth substrate and nanowire structure. Therefore, this feature is particularly important for developing highly efficient optical devices using NWs on low-cost and large-area Si substrates or glass-based poly-crystalline silicon (poly-Si) thin films. These substrates have matured processes which have been applied to form Si-based integrated circuit chips or glass-based flat-panel displays (FPD). Especially using poly-Si is expected to decrease the cost of materials for LED structures comparing with conventional LED structures using compound semiconductor substrates. Moreover, these substrates have good compatibility with mass production process for FPD. However, until now there are no reports on the growth of NWs on poly-Si and their device applications. We report here on the growth of GaAs NWs on poly-Si in relation to the growth conditions and the crystalline of poly-Si.

2. Experimental

As a poly-Si substrate, a 50-nm-thick layer of poly-Si thin film was deposited on a 300-nm-thick SiO_2 coated Si(001) substrate using RF sputtering. This thick SiO_2 layer coated Si(001) substrate is used as an equivalent structure to a glass substrate. We changed the substrate temperatures (T_S) during deposition of poly-Si from room temperature (RT) to 600 °C. After that, a 20-nm-thick SiO_2 layer was formed on the poly-Si thin film by thermal oxidation, and the layer was partially removed using electron beam lithography and wet chemical etching to form periodic mask openings as a template of growth (Fig. 1(A)). The diameter, *d*, of the opening area varied from 60 to 200 nm, and the opening pitch, *a*, of the mask was 500 nm. Using these substrates, GaAs growth was carried out with a horizontal low-pressure MOVPE system. The working pressure was 0.1 atm and the source materials were trimethylgallium (TMG) and arsine (AsH_3). The growth time was 30 minutes. The partial pressure of TMG and AsH_3 were 2.5×10^{-6} atm and 5.0×10^{-4} atm, respectively, which is the normal condition for GaAs nanowires growth on Si(111) substrates. We used three types of the growth temperature (T_G), which were 650 °C, 700 °C, and 760 °C. The grown structures were characterized with scanning electron microscopy (SEM).

3. Results and discussion

SEM images of the grown substrates are shown in Fig. 1 (B)-(D). The GaAs NWs, which had six {-110} sidewall

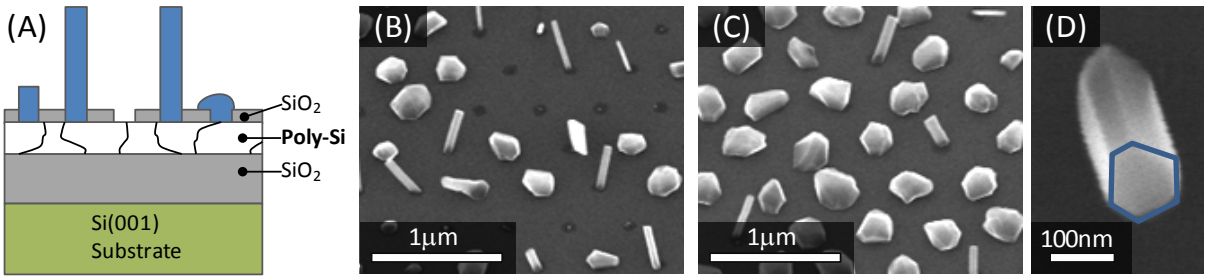

Fig. 1, (A) is a schematic illustration of a cross section of the growth substrate. (B) and (C) are SEM images of birds-eye view of grown substrate with 100-nm and 160-nm diameter under the growth temperature T_G = 700 °C on poly-Si substrate which the substrate temperature during deposition T_S = 300 °C. (D) is the top view of GaAs nanowire.

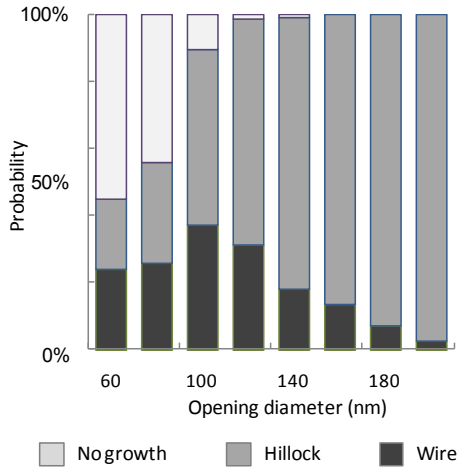

Fig. 2, Occurrence probability of each grown structure dependency on mask opening diameter. T_G and T_S are 700 °C and 600 °C, respectively.

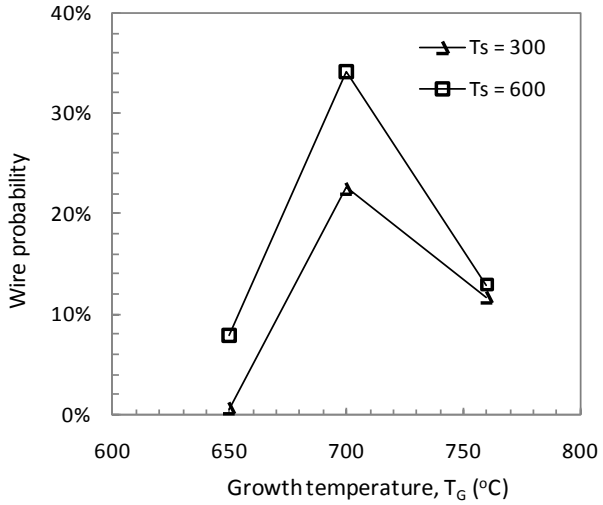

Fig. 4, T_G dependency on probability of wire structures for T_S = 300 °C and 600 °C

facets, were obtained on poly-Si thin films (Fig. 1(D)). Hillock structures and no growth openings were also observed. The occurrence probability for each grown structures as a function of the diameter of the opening (*d*) is shown in Fig. 2. The NWs were mainly observed below *d* = 120 nm. These results indicate that the probability of NWs has strongly dependency on *d*. In a small *d*, the NWs were easy to grow because the opening area most likely had a single-crystalline surface. On the other hand, in a large *d*, hillock structures, which were originated from irregular growth on the grain boundary, were fabricated because the opening area probably had a lot of grains. Moreover, these trends are similar to other substrates, which were grown at other growth temperatures (T_G). Figure 3 shows the probability of wire structures as a function of the substrate temperatures (T_S) during deposition of poly-Si. T_G and *d* were fixed at 760 °C and 100 nm, respectively. The probability

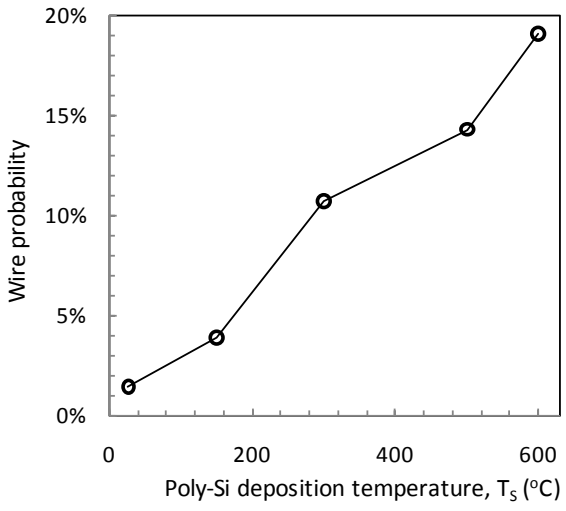

Fig. 3, Probability of wire structures depending on T_S. T_G and d are fixed at 760 °C and 100 nm, respectively.

of wire structures increases as T_S increases, because the grain size of poly-Si is enlarged at higher T_S. As a result, the opening area most likely had a single-crystalline surface even if the same *d*. The probability of wire structures for two different T_S (300 °C and 600 °C) as a function of the T_G is shown in Fig. 4. In all of T_G, the wire probability on the substrate of T_S = 600 °C was higher than that of T_S = 300 °C. In both T_S = 300 °C and 600 °C, T_G dependency shows a similar trend which wire probability decreased in higher and lower temperature side of T_G = 700 °C. This result is consistent with the T_G dependency of the growth rate of GaAs NWs on GaAs(111)B substrate by SA-MOVPE. Therefore, the growth mechanism of GaAs NWs on poly-Si is a same with on GaAs(111)B, which the growth rate of each facets has strongly relationship with growth conditions including T_G [3].

In conclusion, the key parameters for yield of nanowires are the grain size of the poly-Si layer and the growth conditions. In the future, we will consider the optimum growth conditions following the NWs growth mechanism and investigate the poly-Si deposition conditions to enlarge the grain size.

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