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Formation of ohmic contact of InP nanowires without annealing processes

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1. Introduction

Semiconductor nanowires (NWs) have been the next-generation build blocks in optoelectronics, sensing, and electronics [1]. Ohmic contact is an important issue for the device application and it is usually difficult to get good ohmic contacts. One fundamental reason for difficult ohmic contact is the oxides on semiconductor surfaces, which broaden the interlayer thickness and makes it more difficult to transport carriers by the dominant tunneling process. Therefore, annealing has widely been used to obtain good ohmic contact by forming a heavily doped layer, which makes the interlayer thinner, and thus significantly improves the tunneling probability. However, the annealing process results in several disadvantages, e.g., degradation of the NW side surface, interdiffusion of atoms near heterojunction interfaces. It is ideal to form ohmic contacts without using any annealing processes. One effective way is to remove the oxides just prior to the deposition of electrode metals in the high-vacuum chamber without exposing the NW into oxygen-rich environment. InP NW-based nanostructures have shown a promising future. In this report, we studied the formation of ohmic contact of InP NWs without using any annealing processes.

2. Experiments and results

Experiments

We synthesized InP NWs via the Au-catalyzed vapor-liquid-solid (VLS) mode in a MOVPE system [2]. Size-selective Au colloidal particles were dispersed on substrates by spinning-coat method to catalyze the NW growth. We dispersed the InP NWs from the as-grown sample onto SiO2/Si substrates and fabricated field effect transistor (FET) devices by making metallic contacts using photolithography technique [3]. We used the Ar ion sputtering technique to remove the surface oxides by etching a thin layer on the NW surface just prior to the deposition of electrode metals (Ti/Al) in the same high-vacuum chamber. The point of the process is no exposure of the etched NW surface into the air, which normally results in quick formation of an oxides layer, before metallic deposition. To examine the effect of the sputtering, we also fabricated the FET devices without the sputtering process under same other conditions and compared their electrical properties. We performed the electrical measurement on a probe station system using a semiconductor parameter analyzer at temperatures of 300 K (RT) and 19 K.

Results and discussion

InP NWs are vertically aligned on a InP (111) substrate (Fig. 1a), indicating that they were epitaxially grown on the substrate. The InP NW exhibits a tapering shape, which is typically induced by the growth on the NW side faces (Fig. 1b). The NW has a dominant wurtzite structure and <0002> growth direction (Fig. 1c).

For the FET devices with InP-NW-conduction channels, we used the back-gate FET structure (Fig. 2a). Figure 2b shows a typical SEM image of the FET device with a single InP NW between the Ti/Al electrodes. We examined the contact performance by making electrical measurements. We found out that ohmic contacts were obtained when using the Ar ion sputtering method (Figs. 3a and 3b). Furthermore, the ohmic contact behavior remains at a temperature down to 19 K (Fig. 3c). These results indicate that the removal of the surface thin layer, which consists of the surface oxide layer, just before metallic deposition is very effective to improve the contact performance.

We vary the channel conductance using the back gate. The device shows an Ion/Ioff ratio as high as 10^7 at 19 K (Fig. 3d). We believe that this is because the degradation of the conduction channel was prevented by avoiding the annealing step in the fabrication process. To examine the effect of the Ar ion sputtering, we studied the FET structure by TEM measurement (Figs. 4a, 4b, 4c). The difference of 4 nm between the two interfaces, the NW and the underlying SiO_2 layer, the electrodes and the underlying SiO_2 layer, indicates that the surface of the NW-FET device was etched by the Ar ion sputtering and the surface oxide layer was also etched just prior to the metallic deposition.

3. Conclusions

We formed the ohmic contact of InP NWs without using any annealing processes and the device shows good electrical performance. This was achieved by the combination of Ar-ion-sputtering technique and metallic deposition in the same high-vacuum chamber. Our result makes it possible to fabricate InP NW-based optical and electronic devices with high-performance conduction channels.

Acknowledgements

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References

[1] Huang, Pure Appl. Chem. 76 (2004) 2051.

[2] Tateno, et al., Nano Lett. 8 (2008) 3645.

[3] Zhang, et al., J. Phys. Chem. C 115 (2011) 2923.

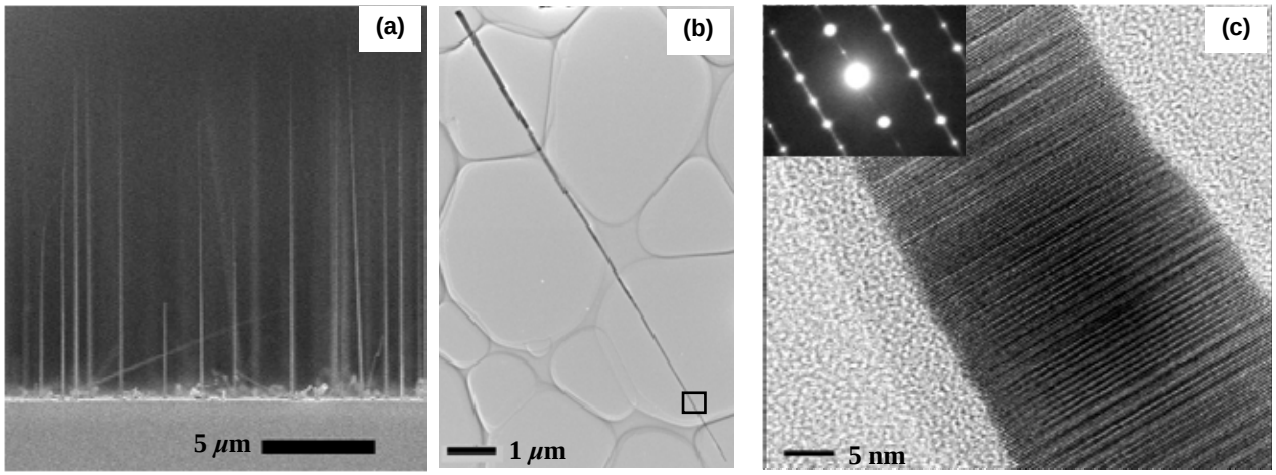

Fig. 1 (a) Cross-sectional SEM image of InP NWs epitaxially grown on a InP (111) substrate. (b) TEM image of a InP NW dispersed on a copper grid. (c) The HRTEM image of the rectangular region near the NW tip drawn in (b). The inset in (c) is the SED pattern, indicating the NW is dominated by the wurtzite structure with the <0002> growth direction.

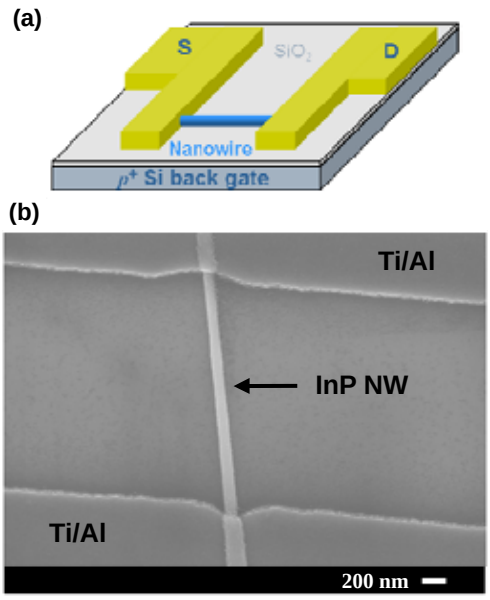

Fig. 2 (a) Schematic diagram and (b) SEM image of a FET device with an InP NW channel on a SiO_2/Si substrate.

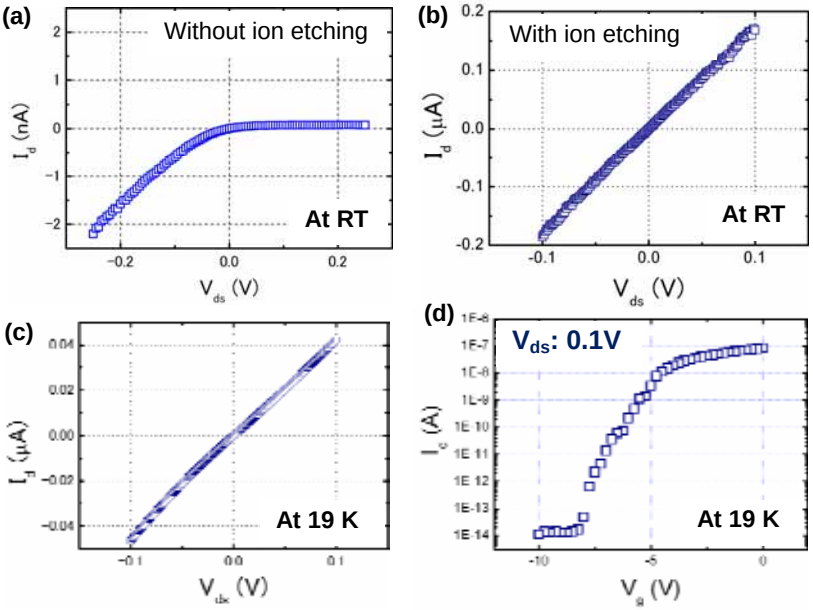

Fig. 3 Typical Id-Vd characteristics of InP NW-FET devices. (a) Without and (b) with Ar ion sputtering at RT. Typical (c) Id-Vd and (d) Id-Vg characteristics of the device with the sputtering process at 19 K.

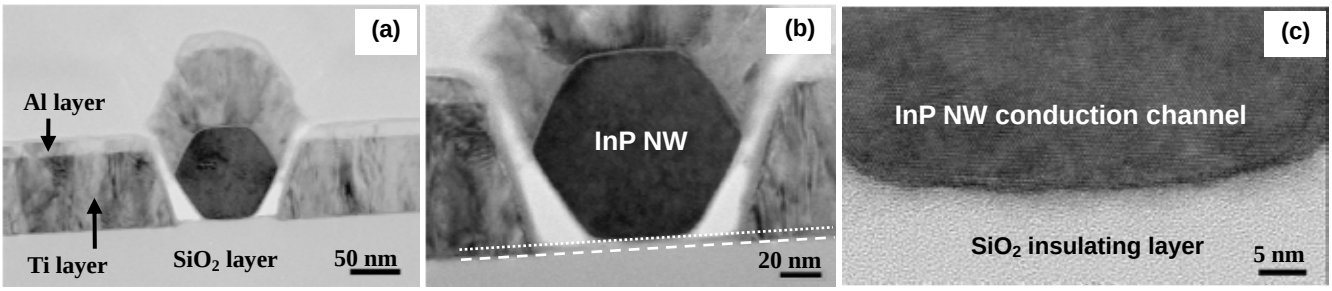

Fig. 4 (a) and (b) Cross-sectional TEM images of InP NW-FET devices with the Ar ion sputtering step. The dotted (dashed) line indicates the interfaces between the NW and the SiO_2 layer (between the electrodes and the SiO_2 layer). (c) HRTEM image of the interface between the InP NW and the underlying SiO_2 layer.