Extended Abstracts of the 2011 International Conference on Solid State Devices and Materials, Nagoya, 2011, pp478-479

Effect of the Drain Configuration on the Current-Voltage Characteristics of Vertical Nanowire Field Effect Transistors

Shreepad Karmalkar, Vijaya Kumar Gurugubelli and K. R. K. Maheswaran

EE Dept., IIT Madras, Chennai 600 036, India; Phone: +91-9445909061 Fax: +91-44-22574402 email: gvk@smail.iitm.ac.in

1. Introduction

Nanowire Field Effect Transistors (NW FETs) are claimed to offer better performance than their planar counter parts [1] and are compatible with existing CMOS technology. Recently [2], we investigated the effects of ambient field from the gate and drain electrodes on the current-voltage characteristics of a Vertical (V) NW FET having lightly doped ungated NW length, L_{DG} (see Fig. 1). In the present paper, these effects are clarified on the basis of Gauss's law and their ramifications on the design of a VNW power FET are detailed.

2. Effects of the Drain Configuration

Refer to Fig. 1 and Table I for the symbols and description of device parameters. The values of these parameters correspond to the experimental device considered in [3]. The effects of our interest originate from the 3D nature of electric field at drain (see Fig. 2). Assume cylindrical coordinate system in which the z-axis coincides with the NW axis and is directed from source to drain, and the r axis is along the NW radius. For a device with $L_P = 0$, we showed the following in [2]: the field component E_r enhances the hole concentration over L_{DG} (see Fig. 3(a)); the ambient field divides L_{DG} into a gate controlled section $(1-\alpha)L_{DG}$ and a drain controlled section αL_{DG} (see Fig. 3(b)); the gate controlled section adds to the channel length; at high $|V_{DS}|$, i.e. in saturation, the field component E_z spreads over the drain controlled section (see Fig. 3(c)); α increases as L_E is increased, leading to higher saturation current, I_{Dsat}, saturation voltage, V_{Dsat}, breakdown voltage, V_{Dbr} and output resistance, R_{out} (see Fig. 3(d)).

In saturation, the spreading of E_z over αL_{DG} simultaneously with the enhancement of the hole concentration in the same region appears to be an anomaly, considering the familiar 1D p-n junction where the spreading of the field is associated with depletion of mobile carriers. An insight into this anomaly is now provided using Gauss's law, written as

$$\nabla .E = \frac{1}{r}\left[\frac{\partial(rE_r)}{\partial r} + \frac{\partial E_\theta}{\partial \theta} + \frac{\partial(rE_z)}{\partial z}\right] = \frac{\rho}{\varepsilon_s} \qquad (1)$$

Assuming uniform conditions over θ, we can write E_z as

$$\frac{\partial E_z}{\partial z} = \frac{\rho}{\varepsilon_s} - \frac{E_r}{r} - \frac{\partial E_r}{\partial r}. \qquad (2)$$

Spreading of the electric field implies reduction of $\partial E_z/\partial z$. Consider the RHS of (2) and refer to Fig. 2. For L_E = 550 nm, E_r is directed outward and increases with r, i.e. the terms E_r and $\partial E_r/\partial r$ are positive and tend to reduce $\partial E_z/\partial z$ implying spreading of the field. However, outward E_r originates from a positive ρ in the wire and so, implies an increased hole concentration as well. Thus, spreading of the field and increased hole concentration occur together for large L_E. In contrast, for a 1D p-n junction, the Gauss's law would not contain the 2nd and 3rd terms of the RHS of (2), and so, increase in ρ would imply an increase in $\partial E_z/\partial z$. Also note that, for L_E = 0, E_r and $\partial E_r/\partial r$ are negative resulting in high $\partial E_z/\partial z$.

3. Design of the Drain Configuration in a VNW power FET

A relatively high power FET may be realized using several VNW FETs, which have a lightly doped L_{DG} and are connected in parallel by a common drain contact realized using a continuous top metal, for increasing the current levels. In such a device, each VNW FET has an inherent drain contact extension, and so, the drain contact not only sums up the currents of individual FETs but also improves the I_{DS}-V_{DS} curve of the whole device, by raising the V_{Dbr}, V_{Dsat}, I_{Dsat} and R_{out} of individual FETs.

Compare the V_{Dbr} from the simulated I_{DS}-V_{DS} curves in Fig. 4 for L_{DG} = 265 nm and 665 nm. The increase in V_{Dbr} with L_{DG} for L_E = 0 is much smaller than that for L_E = 550 nm. Thus, an ungated length raises V_{Dbr} significantly only when it is accompanied by appropriate L_E. It is important to know just how much L_E is sufficient for improving the I_{DS}-V_{DS} curves, because the interwire separation = 2(L_E + wire radius) decides the current density. In Fig. 4, for L_{DG} = 265 nm (665 nm), the I_{DS}-V_{DS} curves for L_E = 120 nm (180 nm) and 550 nm (550 nm) are almost identical. This implies that the field modulation of L_{DG} and the consequent improvement in characteristics are fully manifest using a minimum L_E which is = $L_{Emin} < L_{DG}$ and increases with L_{DG}; increase in L_E beyond L_{Emin} does not fetch much improvement in V_{Dbr}, V_{Dsat}, I_{Dsat} and R_{out}.

The values of L_{DG} and L_E for realizing a VNW power FET of a given V_{Dbr} having the maximum drain current density are obtained from simulation in two steps. First, we obtain the L_{DG} which gives the required V_{Dbr} for $L_E = L_{DG}$. Next, for this value of L_{DG}, we reduce the L_E until the simulated V_{Dbr} starts falling. If process constraints leave a larger L_{DG} than above, the target L_{DG} may be achieved by increasing the conductivity of the NW length, L_P (see Fig.1), by either heavy doping [4] or metal silicidation [5] as done in case of small signal applications. Our simulations show that the device characteristics depend on L_{DG} and L_E alone and not on L_P (see Fig. 5(a)), as the simulated potential contours over L_{DG} within the NW for devices with and without L_P are almost identical if their L_{DG} are the same (see Fig. 5(b)). A detailed design procedure for estimating all the geometrical and process parameters for a specified voltage and current rating will be dealt with in a fuller paper.

References

[1] Q. Li, X. Zhu *et. al.*, Nanotechnology, **20**, 415202 (2009).
[2] S. Karmalkar *et. al.*, Appl. Phys. Lett., **98**, 063508 (2011).
[3] J. Goldberger *et. al.*, Nano Lett., **6**, 973 (2006).
[4] B. Yang *et. al.*, IEEE Electron Device Lett., **29**, 791 (2008).
[5] W. M. Weber *et. al.*, Nano Lett., **6**, 2660 (2006).

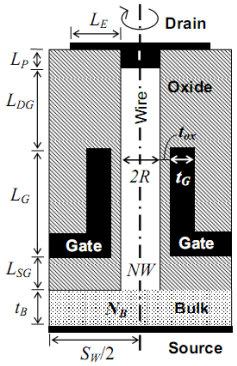

Fig. 1 The cross-section of the silicon VNW- MOSFET considered in our work (diagram not to scale). Top contact is schottky type [3], bulk contact is ohmic.

Table I Details of parameters employed in our simulations. See Fig. 1 for the device structure. Interface charges are neglected [3].

Description	Symbol	Value
Wire – doping (p-type), diameter, separation	N_W, $2R$, S_W	3 x 10^{16} cm^{-3}, 25, 1125 nm
Gate – length, oxide thickness, metal thickness	L_G, t_{ox}, t_G	550, 35, 30 nm
Bulk – doping (p-type), thickness	N_B, t_B	3 x 10^{19} cm^{-3}, 20 nm
Bulk – gate separation, Top contact – gate separation	L_{SG}, L_{DG}	35, 65 – 665nm
Top contact – lateral extension, penetration into the wire	L_E, L_P	0 – (S_W/2 - R) 0 – 600 nm
Work function of – gate, top contact	φ_{MG}, φ_{MT}	4.32, 4.50 eV
Low field hole mobility, Critical normal field for mobility degradation, saturation velocity	μ_0, E_C, v_{sat}	6.89 $cm^2V^{-1}s^{-1}$, 100 KV cm^{-1}, 8.37 x 10^6 cms^{-1}

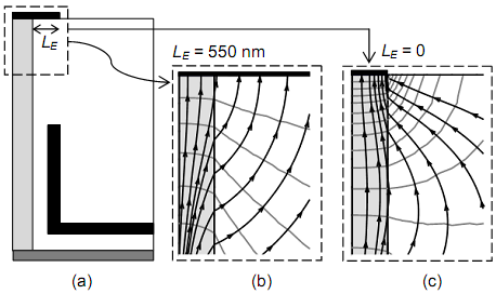

Fig. 2 Schematic of the right half of the cross section of VNWFET with arbitrary L_E (a); Field lines and potential contours (simulated using SENTAURUS) in the dashed box portion of (a) for L_E = 550 nm (b) and L_E = 0 (c). L_{DG} = 665 nm, V_{GS} = -2.5 V, V_{DS} = -5 V.

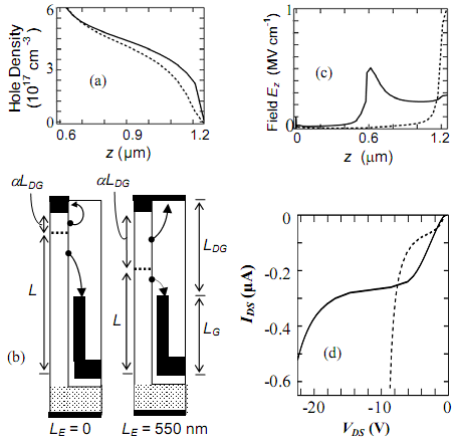

Fig. 3 (a) Simulated hole distribution along the NW axis over L_{DG} from gate edge to drain contact, for V_{GS} = V_{DS} = -2.5 V. (b) Schematic illustrating the division of L_{DG} into drain-controlled and gate-controlled sections, and the effective channel length L, for L_E = 0 and 550 nm. Arrows from L_{DG} represent field lines. (c) Field distribution, E_z, at breakdown along the NW axis from source to drain. (d) Simulated I_{DS}-V_{DS} curves showing linear, saturation and breakdown regions. In (a), (c) and (d) L_P = 0, L_{DG} = 665 nm, V_{GS} = -2.5 V with L_E = 0 (dashed line) and L_E = 550 nm (solid line).

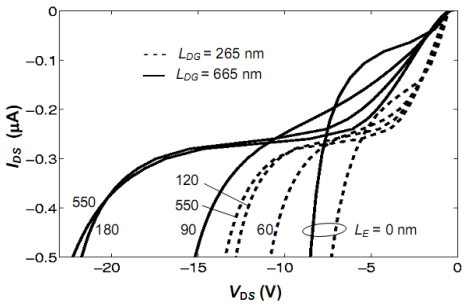

Fig. 4 Simulated I_{DS}-V_{DS} curves for different L_E. See Table I for other parameter values employed in simulation.

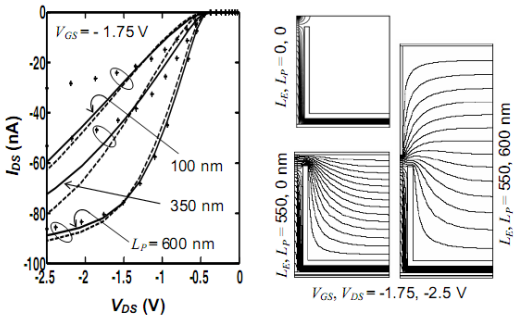

Fig. 5 (a) Solid lines are simulated I_{DS}-V_{DS} curves showing the reduction in the influence of L_E = 550 nm with progressive increase in the drain contact penetration, L_P, and concomitant reduction in L_{DG} = 665 – L_P nm; for comparison, other lines show simulated I_{DS}-V_{DS} curves for devices with same L_{DG} but L_P = 0 and two different values of L_E = 0 (crosses), 550 nm (dashed lines); curves for same L_{DG} are grouped together; solid lines show the reduction in the influence of L_E with progressive contact penetration. (b) Potential contours in right-half of the device cross-section for L_{DG} = 65 nm under different conditions of L_E and L_P.