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Graphene Gated SiO_2 Core-shell Silicon Nanowire Transistors

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1. Introduction

Synthesized silicon nanowires (SiNWs) have been widely studied due to their potential applications to nano-, bio-, and optical-devices [1]. Even though the most convenient way of forming field effect transistor (FET) SiNWs is using simple bottom gates, the all-around gate structure aiming for a better performance requires much more complicated process steps [2].

Recently, the synthesis of large area graphene has become possible by chemical vapour deposition (CVD) [3], and the application of the synthesized graphene on transparent and flexible electrodes has also been popular. This paper presents our first trial of the fabrication and characterization of graphene gated SiNW FETs. In our devices, the SiNWs have core-shell structure with core Si and SiO_2 shell. The graphene covers the top of the SiNW.

2. Experiments

Device Processing

Figure 1 shows a schematic process flow. The SiNW was grown by a standard vapour-liquid-solid (VLS) method [1]. The diameter of the nanowire ranges from 70 to 90 nm. The SiO_2 shell was formed by thermally oxidizing the SiNWs for 30 mins at 800 °C. Figure 2(b) shows a typical transmission electron microscope (TEM) image of the core-shell SiNW exhibiting the shell thickness of 10 ~ 20 nm. The core-shell SiNWs were drop-casted on a silicon substrate with a 100 nm thick Si_3N_4 insulating layer, and source/drain contact opening was performed using photolithography. The SiO_2 shell in the contact area was etched by 6:1 buffered oxide etch (BOE) and the deposition of 30/80 nm NiCr/Au was performed. The subsequent liftoff of the deposited metal resulted in the core-shell SiNW with the source/drain contacts (Fig. 1(f)).

A large area graphene was synthesized on Ni using the condition similar to that in Ref. 3. The Raman spectrum in Fig. 2(a) shows the ratio of D and 2D peak of 1:1, suggesting the successful formation of high quality, multi-layer graphene. The synthesized graphene was transferred on top of the substrate with prepared core-shell SiNWs, and the gate definition was done by photo-lithography and O_2 reactive ion etching (Fig.1 (h) and (i)). Finally, the residual photoresist was removed by acetone. The channel length of the FET was 10 μm, and the length of the graphene gate was 6 ~ 8 μm.

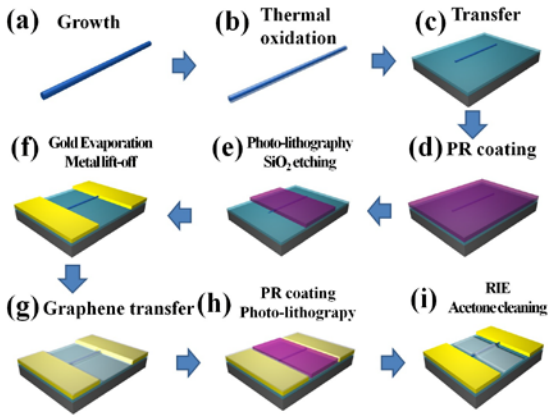

Fig. 1 Schematic process sequence of the graphene gated SiO_2 core-shell SiNW FETs.

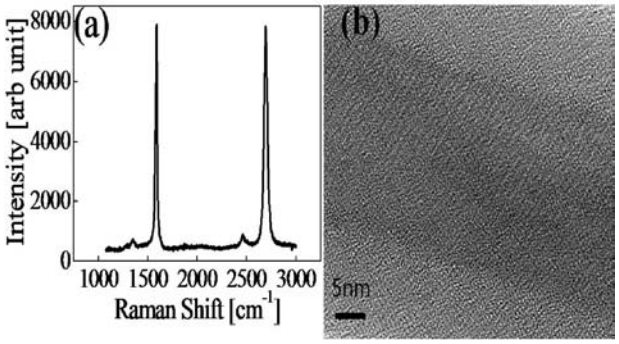

Fig. 2 (a) Raman spectrum of the CVD synthesized graphene. (b) TEM image of the SiO_2 core-shell silicon nanowire

Analysis

The performance of the fabricated FET varied according to the shape of the graphene coverage on SiNWs. The FET of Fig. 3 is an example of broken graphene as can be seen in scanning electron micrographs (SEMs) of Fig. 3(b) and (c). Figure 3(a) showed the drain current (I_{DS})-drain bias (V_{DS}) characteristics measured from the device at

the graphene gate bias (V_{GS}) 0f – 5, 0, and 5 V. They showed only a negligible change of I_{DS} at different V_{GS} values.

On the other hand, other two devices exhibited arch-type graphene covering on the top of the SiNWs as shown in Fig. 4(a) and (b), and in Fig. 5(a) and (b). These two devices showed the clear variation of (I_{DS}) with the change of V_{GS}. As shown both in the I_{DS}-V_{DS} (Fig. 4(c) and Fig. 5(c)) and I_{DS}-V_{GS} characteristics (Fig. 4(d) and Fig. 5(d)).

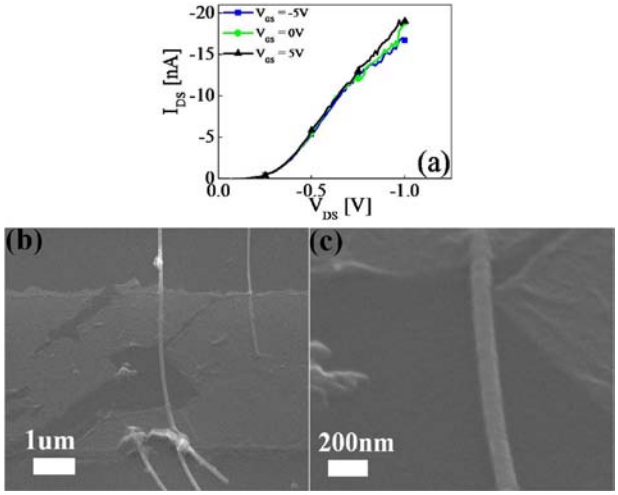

Fig. 3 (a) I_{DS}–V_{DS} measured at V_{GS} values from – 5 V to 5 V. (b) and (c) SEM images of the first fabricated core-shell SiNW transistor ; broken graphene.

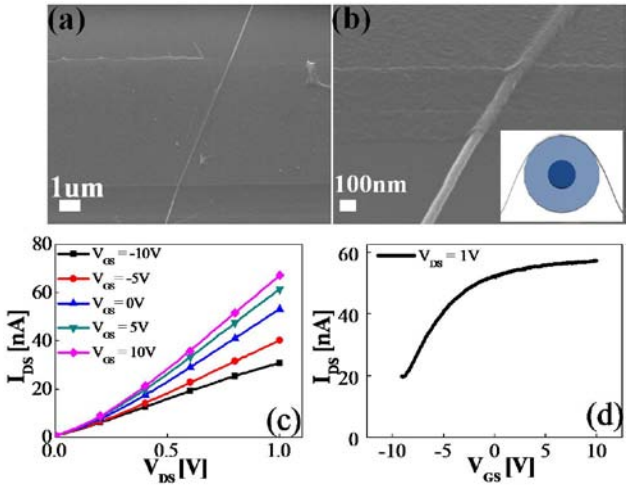

Fig. 4 (a) and (b) SEM images of the second fabricated core-shell SiNW transistor. (inset) Schematic showing the coverage of the graphene gate. (c) I_{DS}–V_{DS} measured at V_{GS} values from – 10 V to 10 V. (d) I_{DS}–V_{GS} at V_{DS} = 1 V.

The transconductance (g_m) of the device in Fig. 4 is 6.80×10^{-9} (A/V), and that of the device in Fig. 5 was 4.58×10^{-9} (A/V). The difference in the gate efficiency observed in the working devices of Fig. 4 and Fig. 5 was related with the relative coverage of the graphene. The insets of Fig. 4(b) and Fig. 5(b) schematically show the situation observed in their corresponding SEM photos. The reason why the graphene gate was lifted and made a smaller coverage in the device of Fig. 5 could be the existence of large impurity introduced on the top of the SiNW during the transfer process.

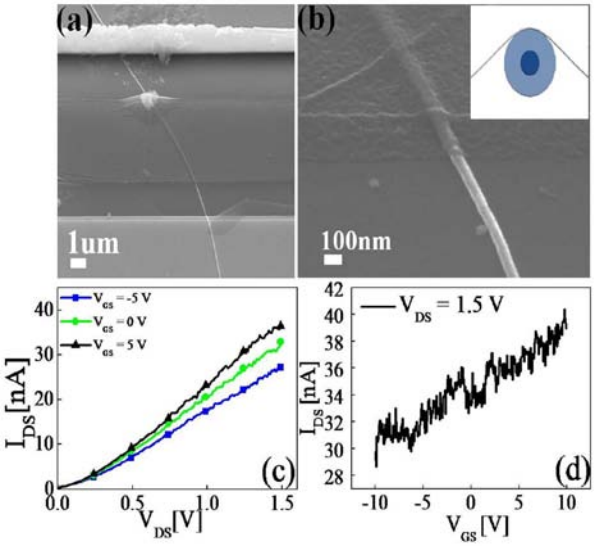

Fig. 5 (a) and (b) SEM images of the third fabricated core-shell SiNW transistor. (inset) Schematic showing the coverage of the graphene gate. (c) I_{DS}–V_{DS} measured at V_{GS} values from – 5 V to 5 V. (d) I_{DS}–V_{GS} at V_{DS} = 1.5 V.

3. Conclusions

The fabrication and characterization of graphene gated core-shell SiNW FETs were presented. The I_{DS}-V_{DS} and I_{DS}-V_{GS} characteristics of three different FETs showed that the device characteristics were closely related with the relative coverage of the graphene gates. Present graphene gates cover only a small portion of the periphery of the SiNWs. Much better gate performance is expected by a better coverage which can be realized using a more flexible single layer graphene.

Acknowledgements

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