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Investigation of Hot Carrier Degradation in STI-based High-Voltage LDMOSFETs by a Novel DCIV technique

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1. Introduction

To follow the trend of lower cost and smaller chip size, lateral DMOS(LDMOS) transistors are widely used in variety of areas due to its compatibility with the standard CMOS process[1]. The STI-based LDMOS devices are implemented by adding STI in the drift region[2]. Because of the high drain operation voltage, hot-carrier-induced degradation becomes a major reliability issue in LDMOS transistors[3-4]. Most of STI-based LDMOS studies are focused on the device electrical performance, thus short of reliability information on hot-carrier degradation of the devices[5]. Moreover, due to the complex device architecture the characterization technique and hot carrier degradation mechanism differ substantially from standard CMOS devices [6-7]. In this paper, a novel direct current IV(DCIV) technique was demonstrated. Through the proper biasing setup, the DCIV current have multiple sharp peak signals, and each peak signal corresponds to a different part of the devices. Comparing the pre- and post-stress DCIV currents, we are able to identify the locations and properties of interface states in the device under hot-carrier stresses. A 2D device simulator is performed to analyze the dependence of device degradation characteristics on interface state position and hot-carrier stress condition.

2. Device Structure

Fig.1 shows a cross-sectional view of an STI-based NLDMOS device studied in this paper, which is implemented in a 0.18μm SOI CMOS compatible BCD process. The device has a net channel length and width of 0.6μm and 20μm, respectively. The off-state breakdown voltage is above 60V. The on-state breakdown is in excess of 40V up to Vgs=5V.

3. Multi-region DCIV Technique

The direct-current current-voltage (DCIV) technique[8] has been used for measuring stress-induced interface traps in standard CMOS devices. In our setup, the source/drain to substrate junction was forward biased with 0.5V, the substrate current Isub was measured when gate voltage was swept from accumulation to slight inversion. As predicted by the Shockley-Read-Hall(SRH) theory, the DCIV peak height above the baseline was approximately proportional to the effective interface trap density, and the peak height is exponentially proportioned to forward bias voltage, shown in Fig.2. Also a double-peak curve was observed from a fresh STI-based LDMOS.

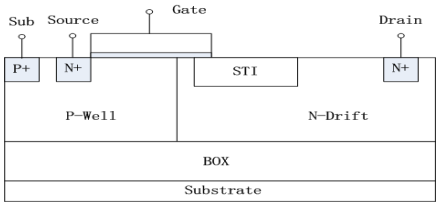

Fig.1 A cross section view of STI-based LDMOS

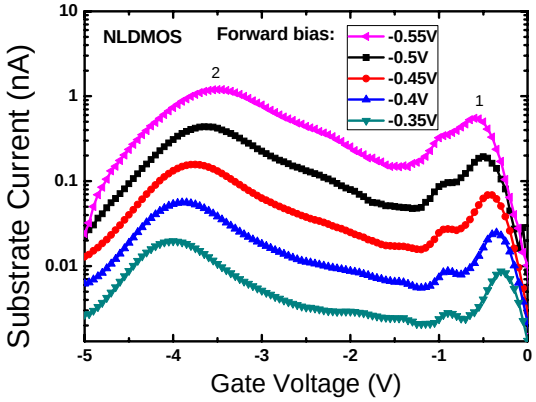

Fig.2 A typical DCIV current spectral

4. Results and Discussion

For understanding typical DCIV spectral, 2D device simulation was conducted by ISE DESSIS tool. The dependence of DCIV current on a single-energy-level interface trap at different locations was simulated(Fig.3). Three distinct DCIV current peaks were obvious, corresponding

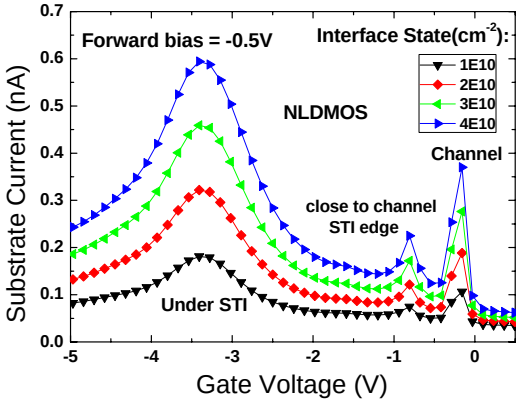

Fig.3 DCIV current simulation results

to channel, close-to-channel STI edge and under STI interface, respectively. The DCIV peak current is proportional to the trap density irrespective of trap locations. The contribution on the linear drain current shift due to those interface states is shown in Fig.4. Idlin degradation induced by the channel interface state is negligible, because the drift region equivalent resistance is the dominant contribution to

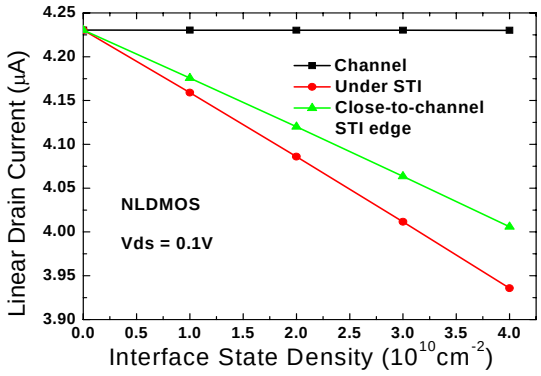

Fig.4 The linear drain current shift by interface state

the device on-resistance. The close-to-channel STI edge and under STI interface state degrades the Idlin linearly.

Compare to the multiple level charge pumping(CP) technique[9], the novel DCIV technique is ease to implement without using the pulse generator, and avoids the potential gate oxide degradation during multiple level charge pumping measurement with high voltage bias.

The maximum substrate current (Vg=2V, Vd=22V, Vs=Vb=0) and maximum gate voltage (Vg=5V, Vd=22V, Vs=Vb=0) stresses were applied to NLDMOS. The impact ionization rate distribution was simulated under two stress conditions(Fig.5). The highest impact ionization was observed at channel and drift region junction close to STI edge corner. The Vg,max stress demonstrated a wider dis-

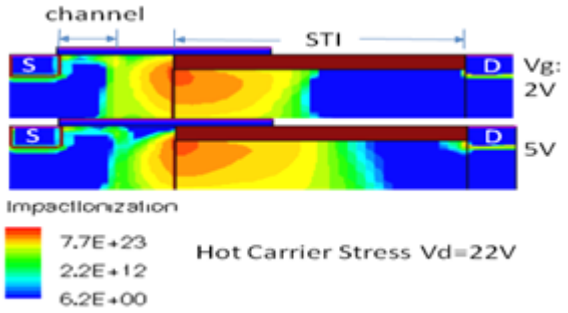

Fig.5 Impact ionization rate distribution.

tribution under STI region. The shift of DCIV current after 5000s stress was summarized in Fig.6. Vg,max stress yielded larger degradation in both channel and STI regions. However, CP and Idlin evolution(Fig.7) demonstrated different trends. Unlike Idlin degradation, the CP current shifted toward the same direction under two stresses. After 5000s stress, the change of CP current under Vg,max stress was about 7x larger than that of Isub,max stress, which indicated higher channel interface states generation. The channel interface states induced by Vg,max stress did not impact on-resistance a lot. Therefore, in term of the on-resistance degradation, the Isub,max stress leads to the worst hot-carrier degradation in an STI-based nLDMOS. Since the on-resistance was dominated by n-drift region, the silicon/STI interfaces should be considered carefully for STI-based LDMOS devices.

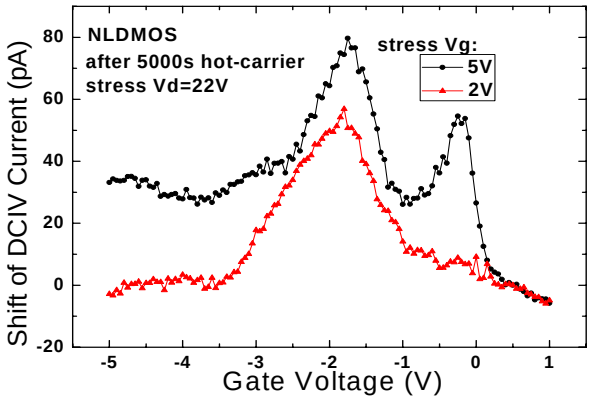

Fig.6 DCIV current after 5000s hot carrier stresses.

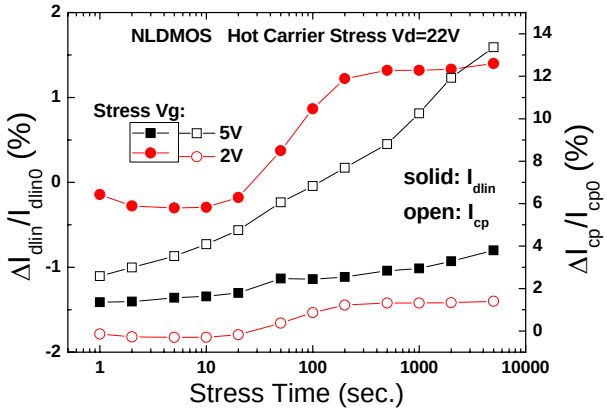

Fig.7 Linear drain and CP current evolutions.

5. Conclusions

A novel DCIV technique was proposed to characterize interface states in each region of an STI-base nLDMOS. The impact of the interface state location on device performance has been analyzed. A correlation between device degradation and DCIV signal has been verified by 2D device simulation and reliability experiments. Our study reveals that Idlin degradation is mainly affected by interface state in the STI region. Our study also shows that maximum Isub stress results in the worst hot-carrier degradation in an STI-based nLDMOS in term of the on-resistance degradation, which is attributed to interface state generation under STI region.

Acknowledgements

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