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High accurate TCAD calibration methodology realizing smart-design of integrated power devices consisting of lateral-IGBT & Diode in SOI micro-inverters

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1. Introduction

High voltage SOI micro-inverter has been widely applied to small power three phase motor drivers in consumer electronics up to 500V 3A ratings [1, 2]. Performance of the micro-inverter IC is mainly determined by integrated power devices, i.e. lateral-IGBT (LIGBT) and lateral-Diode (LDiode). In order to apply the SOI micro-inverter IC to various motor drivers in high voltage automotive electronics, TCAD is appropriate for such characterization and optimization in process & device development of the lateral power devices [3, 4].

We have successfully built a high accurate TCAD calibration methodology providing smart-design tool for integrated SOI LIGBT and LDiode by means of skillful combination of process, device, and mixed-mode circuit simulations.

2. Calibration methodology

2-1. Target devices

SOI-LIGBT (14-cells in parallel, 600V 3A ratings) and LDiode (4-cells in parallel, 600V 3A ratings), fabricated by 0.6μm SOI Bipolar-CMOS-DMOS process, were utilized for the target devices as shown in Fig. 1(a), (b). Fig. 2 shows schematic cross-sectional structures of the SOI-LIGBT and LDiode. Thicknesses of silicon and buried oxide layers are 15μm and 6μm, respectively.

2-2. Concept and tools

Fig. 3 shows **our concept of calibration methodology from process to device parts including DC (quasi-stationary simulation) and AC (transient simulation) modes.** Process and device calibrations were performed by *SPROCESS* and *SDEVICE* which operate on *Sentaurus WorkBench* (SWB) [5]. The calibration methodology is based on the use of straightforward simulation templates on SWB to reduce the effort required by the TCAD users.

2-3. Process calibration

1D and 2D process calibrations were performed by referring measured data of SIMS for doping profiles and SEM for micrographic structures. Double diffused MOS channel region was carefully calibrated by applying three-phase-segregation model [6]. Fig. 4 shows the SOI-LIGBT structure after process calibration.

2-4. DC device calibration

Fig. 5(a) shows $\log(I_C)$-V_G curves of SOI-LIGBT before and after calibration compared with the measured curves. Since $\log(I_C)$-V_G curve strongly depends on both structure and doping profile at channel region, **the discrepancy between simulated and measured values were took back to process calibration** as shown in Fig. 3. The relative error in threshold voltage, Vt, was improved well from -0.15V to zero.

Fig. 5(b) shows simulated I_C-V_{CE} output curves before and after calibration compared with measured curves. The simulated curves were mainly determined by two factors. One is electric-field-dependent mobility model in the inversion layer [7], the other is surface recombination velocity at silicon/oxide surface [8]. By the DC calibration with optimized parameters, relative error in saturation current was improved to 5%. Other DC characteristics such as breakdown and C-V were well calibrated, too.

2-5. AC device calibration

AC device calibration was performed using resistive-load and inductive-load mixed-mode models as shown in Fig. 6. In the figure, all stray inductances (designated by small symbol) were neglected at the beginning of AC calibration.

Fig. 7 shows calibrated turn-off and turn-on waveforms of SOI-LIGBT compared with measured waveforms. In Fig. 7(a), relative error of V_{CE} rise time remained as large as -40% (=0.8μs/1.3μs). In Fig. 7(b), gate voltage peak of 4.4V appeared at 1.6×10^{-7} sec. **The cause of the gate voltage peak was attributed to emitter stray inductance, L_E**, as shown in Fig. 6(a). After AC calibration considering L_E (=20nH), the gate voltage peak of 4.4V was obviously re-appeared in the simulated waveform.

Finally, Fig. 8 shows simulated inductive-load turn-on waveforms of SOI-LIGBT & LDiode system after AC calibration compared with measured waveforms. In Fig. 8(a), the measured gate voltage peak of 3.7V at 2.012×10^{-5} sec was re-created as 4.2V at 2.010×10^{-5} sec, resulting in relative error of only +14%. In Fig. 8(b), relative errors in recovery peak current, I_{RM}, and recovery time, trr, have successfully decreased to -14% (=-1.8A/-2.1A) and -17% (=0.10μs/0.12μs), respectively.

3. Conclusion

By means of the newly developed calibration methodology for SOI-LIGBT and/or LDiode system, **we have attained high accurate TCAD simulations as <±10% and <±20% in relative error, respectively**. Therefore, the design of SOI micro-inverter IC with LIGBT

and LDiode will be hopefully well-designed without any trial and error.

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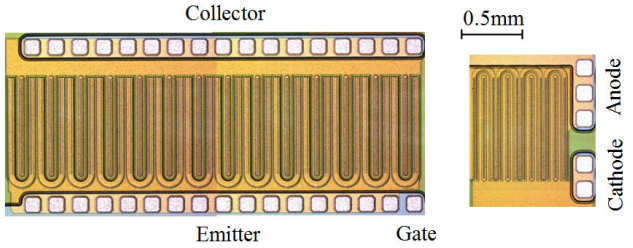
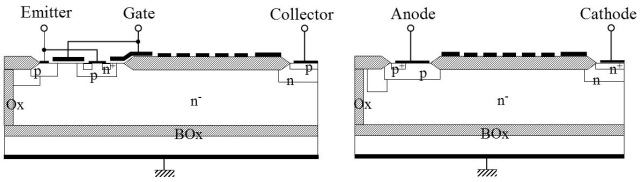
References

[1] A. Nakagawa et al., Proc. ISPSD99, p.321, 1999.
[2] TPD4135K datasheet, 2009.
[3] T. Yamamoto et al., IEEJ Joint Tech. Meeting, EDD-10-93/ SPC-10-150, p.57, Nov. 2010 (in Japanese)
[4] Y. Ashida et al., submitted abstract for SSDM2011.
[5] Synopsys, TCAD Release 2009.06.
[6] Y. S. Oh et al., IEDM Tech. Dig., p.509, 1998.
[7] S. Takagi et al., IEEE Trans on ED, vol. 42, No. 12, p.2357, 1994.
[8] A. Yahata et al., Proc. ISPSD93, p.154, 1993.



(a) SOI-LIGBT (b) SOI-LDiode

Fig. 1 Photos of the fabricated SOI-LIGBT and LDiode chips.



(a) SOI-LIGBT (b) SOI-LDiode

Fig. 2 Schematic cross-sectional device structures.

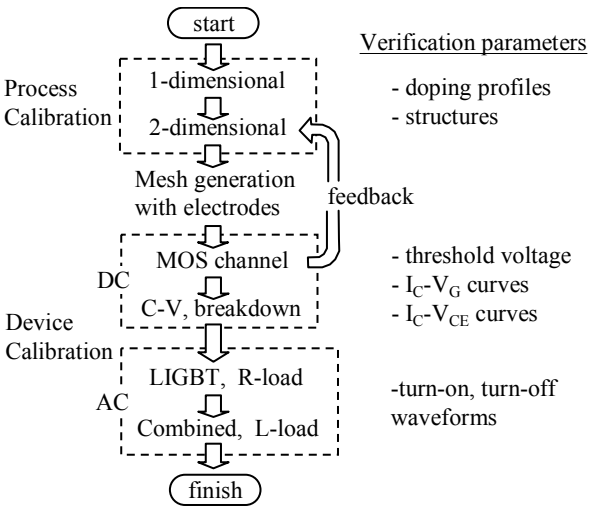


Fig. 3 Conceptual flowchart of the TCAD calibration methodology for SOI-LIGBT & LDiode system.

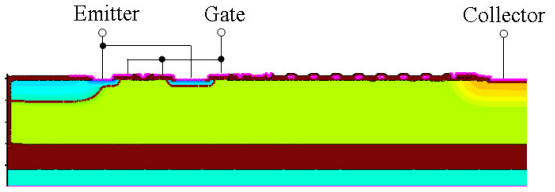
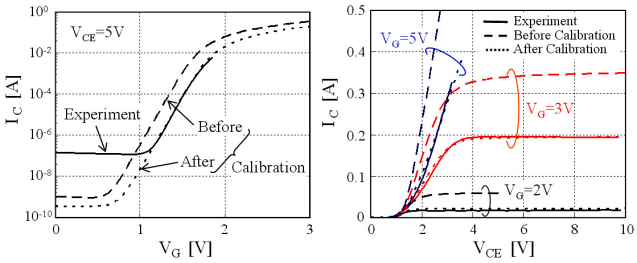
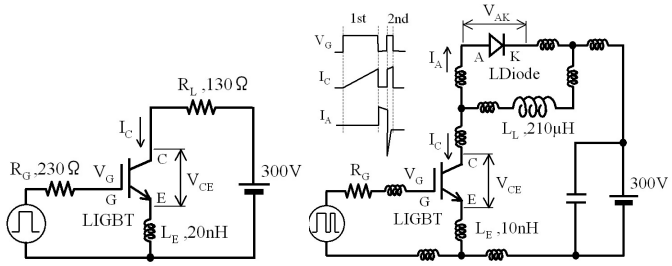


Fig. 4 SOI-LIGBT structure after process calibration.



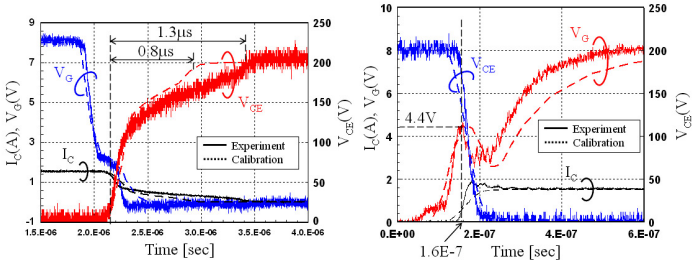
(a) MOS channel characteristics (b) I-V characteristics

Fig. 5 Simulated (a) log(I_C)-V_G (MOS channel) and (b) I_C-V_{CE} (I-V output) curves of SOI-LIGBT before and after DC calibration compared with measured curves. Dashed lines: simulation, Solid lines: experiment.



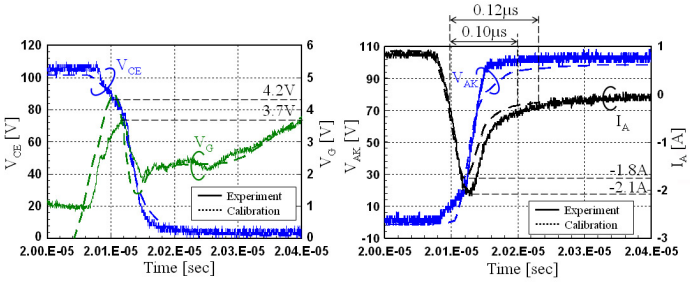
(a) resistive-load model (b) inductive-load model

Fig. 6 Mixed-mode models for AC calibration, (a) resistive-load driven by SOI-LIGBT, (b) inductive-load driven by SOI-LIGBT & LDiode.



(a) turn-off (b) turn-on

Fig. 7 Simulated switching waveforms after AC calibration of SOI-LIGBT using resistive-load model compared with measured waveforms. Dashed lines: simulation, Solid lines: experiment.



(a) SOI-LIGBT (b) SOI-LDiode

Fig. 8 Simulated turn-on waveforms after AC calibration using inductive-load model compared with measured waveforms. Dashed lines: simulation, Solid lines: experiment.