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MIM Capacitors with High Capacitance Density and Low Quadratic Voltage Coefficient by Employing Crystalline-TiO_2/SiO_2 Stacked Dielectric

Chia-Chun Lin, Wei-Yuan Ou, Jia-Rong Wu, Min-Lin Wu, Lun-Lun Chen, and Yung-Hsien Wu*

Department of Engineering and System Science, National Tsing-Hua University, 300, Hsinchu, Taiwan
Phone:+886-3-516-2248 Email: yunhwu@mx.nthu.edu.tw

I. Introduction

Besides a high capacitance density, for high performance metal-insulator-metal (MIM) capacitors, low quadratic voltage coefficient of capacitance (VCC-α or simply α) is also indispensable. According to ITRS, MIM capacitors with a capacitance density of 10 fF/μm^2 and α value less than 100 ppm/V^2 are required by 2016. With the advent of high-κ dielectrics, although MIM capacitors possessing capacitance density higher than 25 fF/μm^2 have been widely explored [1-3], capacitors that concurrently meet the requirement of capacitance density and α value set in ITRS have been rarely reported. Increasing the dielectric thickness is a direct avenue to obtain the desirable α, inevitably, it comes at the price of capacitance density degradation to be less than 10 fF/μm^2 [4-5]. Recently, a stack structure that comprises a HfO_2 film (positive α) and a thin SiO_2 layer (negative α) has ushered in a new approach to achieve low α value without compromising its capacitance density by using the "canceling effect"[6]. Based on this concept, Sm_2O_3/SiO_2 [7] and even HfTiO/Y_2O_3 [8] stacked dielectric have been investigated and show good performance. To further enhance the capacitance density while keeping low α value, in this work, a crystalline-TiO_2/SiO_2 stack was adopted, and a capacitance density of 11.9 fF/μm^2 with α value of 90 ppm/V^2 is achieved.

II. Experiment

Prior to the fabrication of MIM capacitors, 500 nm SiO_2 was grown on Si wafers for better isolation. Then a TaN/Ta bi-layer of 50/150 nm was deposited as the bottom electrode. A TiO_2 film of 14.0 nm was deposited by sputter followed by O_2 furnace annealing at 380 ^oC for 10 min to strengthen its quality by decreasing oxygen vacancies. Thereafter a rapid thermal annealing (RTA) in N_2 at 500 ^oC for 30 sec was performed on some samples to induce phase transition from amorphous to crystalline phase for the TiO_2 film, and this phase transition leads to κ value enhancement from 31 to 111 [2]. Then a thin SiO_2 layer of 2.5 or 7.0 nm was deposited on TiO_2 film by plasma enhanced chemical vapor deposition (PECVD) to study how SiO_2 thickness modulates the α value. Finally, Al of 100 nm was deposited and patterned as the top electrode. **Fig. 1** shows the structure of MIM capacitors and process flow.

III. Results and Discussion

Fig. 2 shows the capacitance-voltage (C-V) curves for MIM capacitors without RTA treatment. As expected, as SiO_2 layer increases from 2.5 to 7.0 nm, the zero-biased capacitance decreases from 7.7 to 3.9 fF/μm^2. Shown in **Fig. 3** are normalized C-V curves and the corresponding α values for these samples. α value of 83 ppm/V^2 can be obtained for samples with 7.7 fF/μm^2 and this performance is comparable to that reported in Sm_2O_3/SiO_2 stack [7]. The change of α polarity from positive to negative sign for samples with thicker SiO_2 suggests that the effect of negative α becomes more prominent. The impact of RTA treatment on C-V characteristics and α value are respectively demonstrated in **Fig. 4** and **Fig. 5**. Under the same physical thickness, samples with additional RTA correspond to a larger capacitance density which is due to the greatly enhanced κ value. As the SiO_2 thickness increases, α has a trend similar to those without RTA. For RTA-processed samples with 2.5-nm SiO_2, a capacitance density as high as 11.9 fF/μm^2 can be obtained while keeping low α level of 90 ppm/V^2. Worth to be mentioned is that, because of low α and high linear voltage coefficient of capacitance (VCC-β) which can be alleviated by circuit technology, normalized C-V curve is unlike a conventional parabolic curve. This capacitance along with α value well exceeds the device requirement in 2016 set by ITRS. Even though the crystalline TiO_2 has extremely high α value [2], the excellent α value for RTA-processed samples can be explained by examining the equation of effective α for a stacked dielectric.

$$\text{Effective } \alpha = \delta_1^3 \times \alpha_1 + \delta_2^3 \times \alpha_2 \ ;$$

$\delta_i \equiv EOT_i/EOT$ where i denotes respective dielectric.

Since the crystalline TiO_2 in samples with RTA contributes very little to equivalent oxide thickness (EOT), δ^3 with extremely low value is obtained and therefore the effect of high α value for the crystalline TiO_2 can be greatly diluted. In addition, the canceling effect provided by SiO_2 also plays the critical role in accomplishing such an excellent device performance. **Fig. 6** shows the dependence of normalized capacitance on measurement temperature and temperature coefficient of capacitance (TCC) of 124 ppm/^oC is observed for RTA-processed samples with 2.4 nm SiO_2. Compared to other dielectrics, as shown in **Fig. 7**, RTA-processed samples with SiO_2 demonstrates the smallest α value in the capacitance density range of interest (10-12 fF/μm^2) for 2016 ITRS requirement and proves the competence of crystalline-TiO_2/SiO_2 stack as the promising dielectric for advanced MIM capacitors. The current conduction mechanism for samples with and without RTA is investigated by plotting the ln(J) versus $E^{1/2}$ curves shown in **Fig. 8** where J and E respectively denote current density and electric field. At low field, the conduction is extracted to follow the Schottky emission model. **Table I** summarizes the major device parameters for MIM capacitors with various electrodes and dielectrics [4, 6-8] and a crystalline-TiO_2/SiO_2 stack shows the most promising characteristics. Note that further improvement is possible by employing a post-RTA NH_3 plasma treatment to well passivate the grain boundary induced leakage paths [9-10] and replacing the low-work function electrode of Al with a higher one to increase the barrier height for carrier injection, both of which are helpful to suppress leakage current.

IV. Conclusion

A crystalline-TiO_2 film is found to have a high κ value of 118. By integrating it with a thin SiO_2 layer which provides the canceling effect of α value as the stacked dielectric, MIM capacitors reveal superior device characteristics to other dielectrics in terms of a capacitance density of 11.9 fF/μm^2 and low α value of 90 ppm/V^2. This stacked dielectric holds great potential to be used in precision analog circuit application beyond 2016.

Acknowledgement

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References

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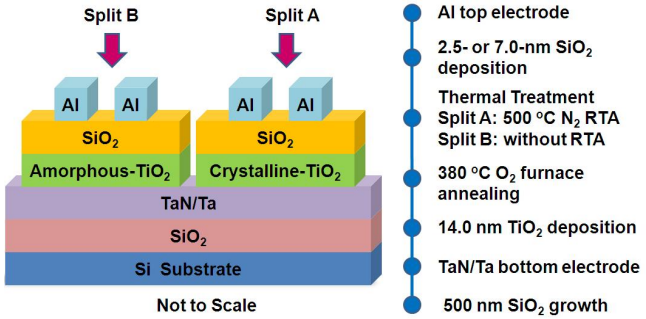

Fig. 1 Structure and process flow of MIM capacitors.

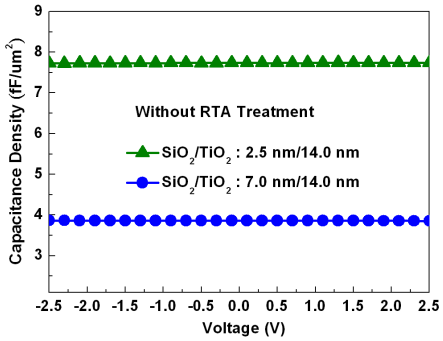

Fig. 2 C-V characteristics for SiO_2/TiO_2 MIM capacitors without RTA treatment.

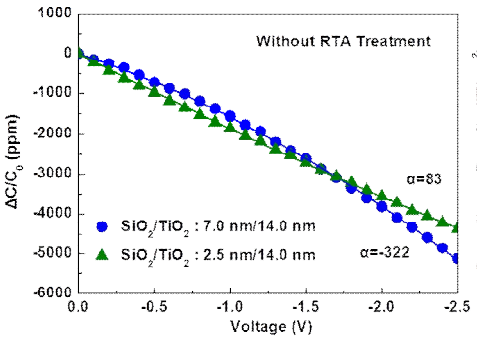

Fig. 3 $\Delta C/C_0$ vs. voltage for SiO_2/TiO_2 MIM capacitors without RTA treatment where C_0 is the zero-biased capacitance.

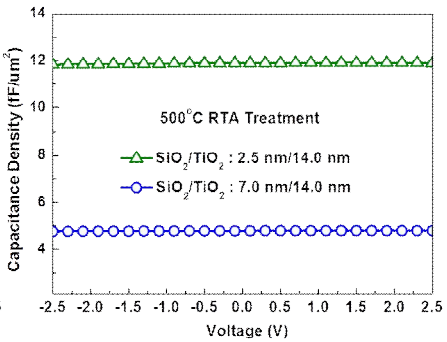

Fig. 4 C-V characteristics for SiO_2/TiO_2 MIM capacitors with RTA treatment.

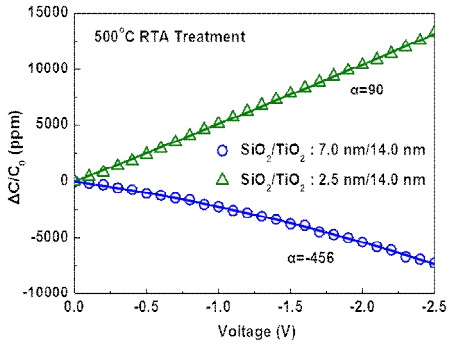

Fig. 5 $\Delta C/C_0$ vs. voltage for SiO_2/TiO_2 MIM capacitors with RTA treatment where C_0 is the zero-biased capacitance.

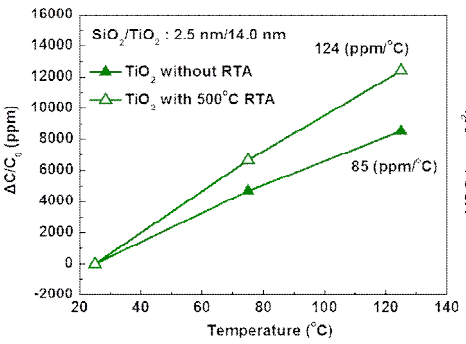

Fig. 6 Temperature-dependent normalized capacitance for MIM capacitors with or without RTA treatment.

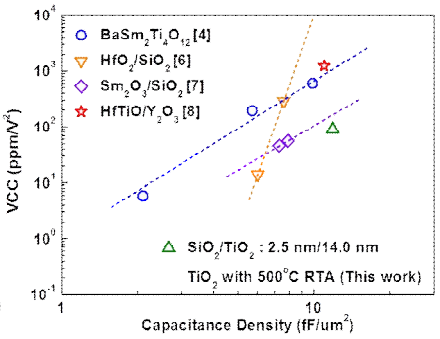

Fig. 7 VCC-α vs. capacitance density for MIM capacitors with various high-κ dielectrics.

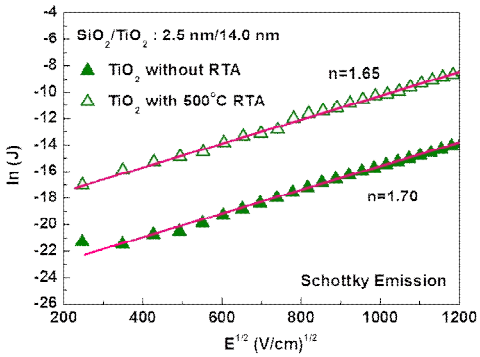

Fig. 8 ln(J) vs. $E^{1/2}$ for SiO_2/TiO_2 MIM capacitors with and without RTA treatment.

Table I. Comparison of MIM capacitors with various dielectrics, top electrodes and process temperatures.

	$BaSm_2Ti_4O_{12}$ [4]	HfO_2/SiO_2 [6]	Sm_2O_3/SiO_2 [7]	$HfTiO/Y_2O_3$ [8]	SiO_2/TiO_2 (Without RTA)	SiO_2/TiO_2 (500 °C RTA)
Process Temp. (°C)	300	420	420	400	380	500
Top Electrode	Pt	TaN	TaN	Pt	Al	Al
Work-function (eV)	5.6	4.6	4.6	5.6	4.3	4.3
Capacitance Density (fF/μm²)	9.9	6	7.3	11	7.7	11.9
VCC (ppm/V²)	599	14	46	1222	83	90