Study of Local Charging Phenomena during SiO₂ Contact Hole Etching

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1. Introduction

Top-down plasma micro/nano processing is increasingly important for a continuous development of ultra large scale integrated (ULSI) circuits. In particular, etching of contact holes through SiO₂ film to Si or silicon nitride layers is a crucial process for the fabrication of multilayer interconnects. Particularly, we have many difficulties in a dry etching of high aspect-ratio contact hole (HARC) which is a crucial step for multi-layer interconnect. According to ITRS roadmap in 2010, contact hole with the aspect-ratio of >20 and the size of a few ten nanometer is required for DRAM fabrication. In the past two decades, etching processes of high-aspect-ratio contact hole (HARC) have caused serious problems, such as RIE-lag, Si recess, etch stop, and breakdown of gate oxide, with a further shrinkage of design rule to sub-nm. A local charge accumulation inside a contact hole during SiO₂ etching is considered as one of the origin of plasma-induced damages (PID).

Reactive ion etching (RIE) of SiO₂ using fluorocarbon gas chemistry proceeds under the competition of surface protection by the deposition of polymer radicals (CₓFᵧ) and chemical sputtering by energetic ions. Under a practical condition, etched surface is always covered with thick polymer layer made of CF radicals. At the same time, sidewall is protected against the energetic ions by polymer deposition. Therefore, the polymer film on the sidewall with finite conductivity has big influence on charge accumulation, resulting in the characteristics of SiO₂ etching.

In this study, charging voltage accumulated in a hole is measured using hole-patterned SiO₂ chip. The charging voltage will be compared with the simulation. Then, we ascribe the voltage difference to the surface conduction on the sidewall due to polymer deposition. Surface conductivity is evaluated as functions of plasma parameters and the aspect ratio of the contact hole.

2. Methodology

2-1. Experiment [1]

Charging voltage measurement system embedded in a two-frequency capacitively coupled plasma (2f-CCP) chamber is shown in Fig. 1. Two types of chips, i.e. hole-patterned SiO₂ chip and blanket Si chip, are set on the electrode biased by the low frequency (LF: 500 kHz) source in order to measure the bottom charging potential of both patterned SiO₂ chip and flat Si chip. A powered electrode driven by very high frequency (VHF: 100 MHz) source is located at the opposite of the LF source. We have prepared hole-patterned SiO₂ chips with different aspect ratios (3, 5 and 10). The patterned chips, measuring 17 mm x 23 mm, had 2.3 x 10¹⁰ holes at a thickness of 1.1 µm. The potential difference on the bottoms between chips was measured as a charging voltage by using a pair of high-voltage probes.

2-2. Simulation [2]

Temporal evolution of the local surface potential inside the geometrically fixed structure was traced by a particle simulation with Poisson’s equation as a function of aspect ratio,

\[ \nabla^2 V(x, z, t) = \begin{cases} 
  -e \frac{n_p(x, z, t) - n_e(x, z, t)}{\epsilon_0} & \text{in gas phase} \\
  -\rho_e(x, z, t) / \epsilon_0 & \text{on SiO}_2 \\
  0 & \text{in SiO}_2 
\end{cases} \]

where \( V \) is the potential, \( n_p \) and \( n_e \) are the number density of positive ions and electrons, respectively. Two-dimensional \((x, z)\) trench structure with periodic boundary was considered in a SiO₂ layer on a grounded Si substrate. The details of the charging simulation can be referred elsewhere [3].

3. Results and Discussion

The comparison of the charging voltages obtained from the experiment and the simulation is shown in Fig. 2 as a function of voltage amplitude of the biased LF electrode, \( V_0 \). In the experimental result (AR = 5), the charging voltage increases almost linearly with \( V_0 \) and then saturates to a value of \( \sim 30 \) V. When a higher \( V_0 \) is applied, a larger sheath potential makes the angular distribution of ions (IAD) narrower, resulting in the charge buildup at the bottom of the hole. The effect of decreasing the width of the IAD, however, becomes small under higher \( V_0 \), presumably \( V_0 > 120 \) V.

On the other hand, the simulated result simply shows a linear increase with increasing \( V_0 \), and finally approaches to several hundred of volts. The difference of both charging voltages \( \Delta V \) implies that the saturation of the experimental charging voltage cannot be explained only by the narrowness of the IAD. Therefore, the surface conduction current on the wall will be a possible mechanism for relaxing the charge buildup at the bottom of the SiO₂ hole. When the...
surface conductivity of CxFy polymer layer on a wall $\sigma$ was taken to be $1.0 \times 10^{-8} \, \Omega^{-1} \text{cm}^{-1}$, the charging voltage at $V_0 = 300 \, \text{V}$ and AR = 5 reduced to 48 V, as also shown in Fig. 2 (◆). This indicates that the optimal value of surface conduction current $J_e$ will be estimated by comparing the experimental and numerical results after fitting $\sigma$ as $\Delta V \sim 0$.

Furthermore, we will investigate the influence of the charging voltage $V_{ch}$ on the underlying gate structure by considering the tunneling current flowing through thin gate oxide ($\sim$ nm). Gate oxide voltage $V_{ox}$ gives the complex behavior as shown in Fig. 3. When the etching progresses and the aspect-ratio of the hole increases, $V_{ch}$ linearly increases and $V_{ox}$ keeps almost the same value. On the other hand, under the condition of aspect-ratio > 7, $V_{ch}$ drastically decreases and $V_{ox}$ gradually increases due to the contribution of the tunneling current.

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**References**


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Fig. 1: Schematic of a two-frequency capacitively coupled plasma (2f-CCP) system, and the arrangement of patterned SiO$_2$ and flat Si chips for measurement of the bottom charging voltage.

Fig. 2: Charging voltage as functions of voltage amplitude of the biased electrode and aspect ratio of the SiO$_2$ hole. Dotted line: experimental, solid lines: simulation.

Fig. 3: Charging voltage at the bottom of the hole $V_{ch}$ and gate oxide voltage $V_{ox}$ as a function of aspect-ratio (right side)