Impact of Aspect Ratio on the Subthreshold RTN Amplitude of Multi-Gate MOSFETs

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Abstract
In this work, we have investigated the impact of aspect ratio on the RTN amplitude (drain current fluctuation) for multi-gate MOSFETs in the subthreshold regime using TCAD simulations. Our study suggests that, for a given total effective width, the multi-gate device designed with lower aspect ratio (e.g., Tri-gate with AR = 1) may exhibit better immunity to RTN than the higher aspect ratio design (e.g., FinFET with AR = 2.5).

Introduction
With the continued development of advanced VLSI technology, MuG-FET has been taken as one of the most promising candidates to extend CMOS scaling. MuG-FET has been demonstrated to have superior gate control, improved electrostatic integrity and device variability for post-22nm technology node [1][7]. However, for future technology generation, the current fluctuation induced by random telegraph noise (RTN) has been regarded as a serious problem [2][6]. Whether various MuG-FET device design will lead to different degree of drain-current fluctuation by RTN has rarely been known and merits examination. In this work, we investigate the impact of aspect ratio (the fin-height to fin-width ratio) on the RTN amplitude for MuG-FET operated in the subthreshold regime (worst case) using TCAD simulations.

Methodology
3-D TCAD simulations [3] were utilized in this study. The simulation methodology for the magnitude of RTN amplitude has already been developed in [4]. We assumed that the trapped electron in the defect state is located at the Si-channel/High-K interface of the MuG-FET device, and the defect is an acceptor-type state. Our assessment focused on the change in the drain current (ΔI_d/I_d) induced by the trapping/de-trapping of a single electron. Fig. 1(a) illustrates the distorted potential contour resulting from a single charged trap at the interface of the transistor sidewall. Fig. 1 (b) shows 5 kinds of aspect ratio (AR) design for the MuG-FET in this study. These devices are all designed with intrinsic channel, L_eff= 15nm, EOT=0.5nm, and the total effective width=60nm.

Results and Discussion
Fig. 2 (a) and (b) examine the dependence of the RTN amplitude (ΔI_d/I_d) at V_g = 0V on the location of individual charged trap across the sidewall interface for MuG-FET with AR=2.5 and AR=1, respectively. Larger RTN amplitude can be found in the middle region between source/drain (i.e., at 0.5L_eff) and ΔI_d/I_d gradually decreases toward source/drain, which is consistence with the previous study for bulk MOSFETs [4]. While considering the trap placed along the vertical direction (y-direction), the largest RTN amplitude occurs for the trap located near the bottom of sidewall channel (~ 0.1H_fin), which is also supported by the electron density contour shown in Fig. 3. In addition, in comparison with the device with AR=1, much larger RTN amplitude for the device with AR=2.5 can be seen from Fig. 2. In other words, for a given total effective width, the MuG-FET designed with lower aspect ratio (e.g., Tri-gate with AR=1) may exhibits better immunity to RTN than the higher aspect ratio design (e.g., FinFET with AR = 2.5).

In the subthreshold region, the RTN amplitude can be expressed as:

\[ \frac{\Delta I_d}{I_d} = \frac{g_m}{I_d} \Delta V_{TH} \approx \frac{2.3}{SS} \Delta V_{TH} - (1), \]

where g_m is the transconductance, SS is the subthreshold swing, and ΔV_{TH} is the trap-induced threshold-voltage shift. Fig. 4 (a) shows the correlation between the RTN amplitude and subthreshold slope for various aspect-ratio MuG-FET devices with a single trap at 0.1H_fin and 0.5H_fin, respectively. It can be observed that the RTN amplitude for MuG-FET with higher aspect ratio shows a similar trend to the subthreshold slope. It indicates that the magnitude of RTN amplitude is mainly determined by the subthreshold slope for devices with higher aspect ratio. Fig. 4 (b) shows that as the RTN amplitude ΔI_d/I_d is normalized with the product of subthreshold slope and ΔV_{TH}, the value is nearly independent on the aspect ratio. It can also be seen from Fig. 4(b) that, in addition to the subthreshold slope, lower ΔV_{TH} also contributes to the observed smaller RTN amplitude for MuG-FET with lower aspect ratio.
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References

Fig. 1 (a) Schematic sketch of a Multi-gate structure and its potential contour induced by a single trap. (b) Device design with 5 kinds of aspect ratio (total effective width =60nm) [5].

Fig. 2 Impact of the trap location on the subthreshold RTN amplitude ($\Delta I_d/I_d$) for MuG-FET with (a) AR=2.5 and (b) AR= 1.

Fig. 3 Electron density distribution of the cross-section sliced at 0.5$L_{eff}$ ($V_g=0V$) for MuG-FET with (a) AR=2.5, and (b) AR=1. The trapped charge is located along a line from $H_{Fin\_top}$ to $H_{Fin\_bottom}$ through the center of the sidewall.

Fig. 4 (a) Relationship of the subthreshold RTN amplitude and subthreshold slope for MuG-FET with a single trap located at $y = 0.1H_{fin}$ and $y = 0.5H_{fin}$, respectively. (b) Verification of Eqn. (1). The impact of AR on $\Delta V_{th}$ is also shown.