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Integration of InGaAs Nanowire Vertical Surrounding-Gate Transistors on Si

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1. Introduction

Semiconductor nanowires (NWs) have attracted a great deal of attention for use in nanometer-scale electronics and optical devices because they have small diameters and large surface areas that enable high-density integration of active devices on various platforms. Recent advances in heterepitaxial techniques, such as vapor-liquid-solid (VLS) method [1-4] and selective-area growth (SAG) [5,6] have enabled integration of III-V compound semiconductor NWs with Si substrates. These materials integrated on Si are expected as building blocks for next-generation Si electronics and photonics, such as a fast channels in vertical nanoarchitectures, steep-slope switches, and optical light sources and detectors on Si. Recently, we have integrated vertically aligned III-V NWs on Si(111) substrate by using selective-area metal-organic vapor phase epitaxy (SA-MOVPE) [7,8], and demonstrated InAs NW-based vertical surrounding-gate transistor (NW-VSGT) [9] and GaAs NW-based light-emitting diodes [10] on Si substrates.

For future transistor scaling, there are emerging challenges in integration of III-V transistors on Si retaining high carrier mobility in the III-V channels. Ternary InGaAs-based metal-oxide-semiconductor field-effect transistors (MOSFETs) are a promising transistor for future n-MOS with low-power and high speed. Recently, InGaAs-based quantum-well FET (QWFET) [11] and multi-gate FinFET integrated on Si [12] have been reported. Non-planar type, InGaAs VSGT, however, have been less investigated because growth method for aligning a vertical InGaAs NWs on Si has been lacked.

Here we present an integration of position-controlled and vertically aligned InGaAs NWs on Si(111) substrate by using SA-MOVPE, and demonstrate a fabrication of highly conductance InGaAs NW-VSGT on Si substrate.

2. Experimental details

2-1. Growth of InGaAs NWs on Si by SA-MOVPE

The substrate was n-type Si(111). After 20 nm-thick SiO_2 was formed by thermal oxidation, openings were formed using electron beam (EB) lithography and wet etching. InGaAs NWs were grown in low-pressure horizontal MOVPE system. Trimethylgallium (TMGa), trimethylindium (TMIn), and arsine (AsH_3) were used for growth materials. The partial pressures of TMGa, TMIn and AsH_3 were [TMGa] = 5.7×10^{-7} atm, [TMIn] = 9.2×10^{-7} atm, and [AsH_3] = 5.0×10^{-4} atm, respectively. Monosilane (SiH_4) was used for n-type dopant. The ratio of [TMIn]/{[TMIn] + [TMGa]} in vapor phase was 0.61. The growth temperature was 670°C and growth time was 20 min. Before the InGaAs NW growth, Si(111) substrate was annealed at 925°C in H_2 and treated in AsH_3 gas to form Si(111) 1×1:As surface [7]. At last, flow-rate modulation epitaxy (FME) was introduced to completely aligned the vertical InGaAs NWs on Si(111) as shown in Fig. 1(a). Fig. 1(b) shows the typical growth results of the InGaAs NWs on Si(111) substrate. The uniformed and vertically aligned InGaAs NWs were grown on Si(111). The average diameter of the InGaAs NWs was 80 nm, and the average height was about 1 μm. EDX line scan profile showed the In composition of the InGaAs NW was approximately 67 ± 2% (not shown here).

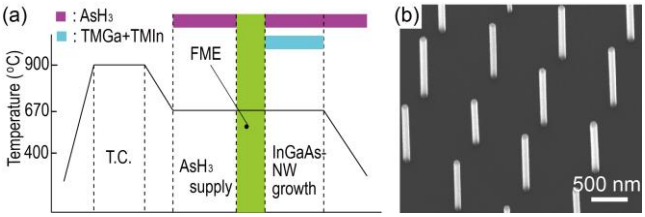

Fig. 1 (a) Growth sequence for integrating vertical InGaAs NWs on Si(111) substrate. T.C. stand for thermal cleaning and FME means flow-rate modulation epitaxy. (b) 30°-tilted SEM image of the InGaAs NWs on Si(111). The diameter of the InGaAs NWs are 80 nm, and height is 1 μm in average.

2-2. Fabrication process for NW-VSGT

After the InGaAs NW growth by SA-MOVPE, InGaAs NWs were covered with $Hf_{0.8}Al_{0.4}O_x$ film by atomic layer deposition (ALD). This oxide was used for gate oxide. The oxide thickness was 12 nm (EOT = 2 nm). Next, tungsten (W) was deposited by RF sputtering. This film was used for gate metal and lithographically defined in NW-grown masks (50×50 μm^2). Then, the NWs were spin-coated by benzoctclobutene (BCB, DOW CHEMICAL) and etched back by reactive-ion etching (RIE) with CF_4/O_2 mixed gas. After these procedures, the W/HfAlO films on top portion of the InGaAs NWs were etched simultaneously. Fig. 2(a) shows SEM image at this procedure. After the RIE, the NWs were spin-coated by BCB, and etched back by RIE. This process was to electrically isolate between gate and drain metals. Ni/Ge/Au/Ni/Au was evaporated onto a lithographically defined region as drain contact. Ti/Al was evap-

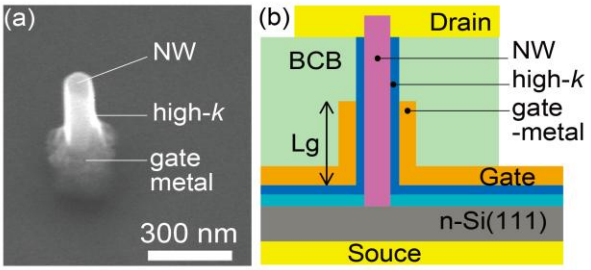

Fig. 2 (a) SEM image of device structure after RIE etching of gate metal and gate oxide. (b) Schematic of a cross-section of the NW-VSGT. The high-k is $Hf_{0.8}Al_{0.2}O_x$ film and gate metal is W film. The drain metal is Ni/Ge/Au/Ni/Au and source metal is Ti/Au. The L_g is 200 nm.

orated on Si substrate as source contact. Detail of this device process is reported elsewhere [9]. The schematic of the NW-VSGT structure is illustrated in Fig. 2(b). In this device, 10 NWs were connected in parallel on a same drain contact pad. The gate length (Lg) was 200 nm. Finally, the NW-VSGT was annealed at 420ºC in N_2 ambient to obtain Ohmic contacts at sour/drain region.

3. Results and Discussions

Electrical properties of the InGaAs NW-VSGT were measured by using parameter analyzer (Agilent, 4156C) at room temperature in dark. The measured current was normalized by using the number of the InGaAs NW and outer perimeter of the InGaAs NW. Fig. 3(a) and (b) shows the output and transfer characteristics of the InGaAs NW-VSGT on Si. Drain current (I_{ds}) was reasonably modulated by gate bias, meaning moderate demonstration of InGaAs NW-VSGT. The switching behavior showed n-type enhancement-mode FET with a threshold voltage (V_{th}) of 0.1 V. The ratio of I_{ON}/I_{OFF} was approximately 10^6, and a minimum subthreshold slope (SS) was 90 mV/dec. The average SS between -0.5 V to + 0.5 V was 120 mV/dec. A maximum drain current (I_{d_max}) was 100 μA/μm at V_{ds} = 1.0 V, and tranceconductance (g_{m_max}) was 130 μS/μm.

The switching behavior of the InGaAs NW-VSGT was significantly improved as compared to InAs NW-VSGT as previously reported [9]. In case of InAs NW-VSGTs on Si substrate, heterointerface of InAs/Si formed band discontinuity, and the discontinuity degrade the device performance. The degradation factor increased series resistance and reduced I_{ds} [9]. Also, misfit dislocation network resulted from a highly lattice mismatch (11.6% in InAs/Si) across the heterointerface [7] seemed to degrade the properties. On the other hand, band discontinuity across the InGaAs/Si were not so pronounced as InAs/Si interface because a current-voltage characteristic at V_{ds} =0 closed to a symmetry curve. Thus, the device performance in the InGaAs NW-VSGT on Si was enhanced.

Moderate SS properties indicated the interface high-*k*/InGaAs has a good property. Capacitance-voltage (C-V) characteristic showed reasonable curve and clear accumulation and depletion behavior (not shown here). The merit of direct integration of the InGaAs NW-VSGT is

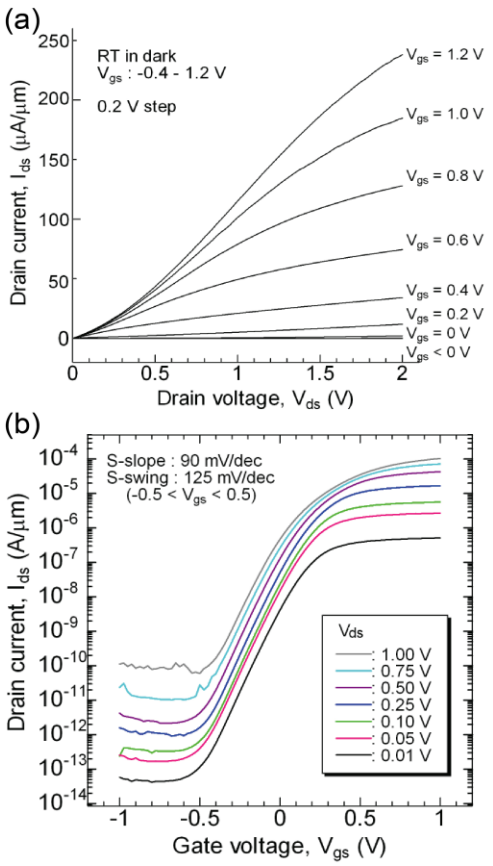

Fig. 3 Electrical properties of InGaAs NW-VSGT on Si. (a) Output characteristic, (b) Transfer characteristic.

capability for ducing Off-state leakage current with a combination of surrounding-gate architecture.

4. Conclusions

We reported on the integration of position-controlled and vertical-aligned InGaAs NWs on Si substrate by using SA-MOVPE, and the fabrication of a vertical NW-VSGT. Moderate switching behavior with highly conductance was observed from the first InGaAs NW-based surrounding-gate structure.

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