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# Body Channel Type Vertical MOSFET to Suppress Gate Leakage Current

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## 1. Introduction

The severely increased power dissipation with gate leakage in CMOS technology owes its origin to conventional scaling limitations of MOS devices. Strong electric field at the gate dielectric increases gate leakage at an exponential growth [1]. Recently, the Surface Channel type Vertical MOSFET (SC-VMOS) shows the excellent device performances [2][3], and has ability to overcome the scaling limitations. This paper proposes a novel Body Channel type Vertical MOSFET (BC-VMOS) to suppress gate leakage current. It is demonstrated that BC-VMOS with 50nm pillar can suppress gate leakage current density by 54% with keeping excellent driving current and sub-threshold leakage performances in comparison with the conventional SC-VMOS.

## 2. Concept of Body Channel Type Vertical MOSFET

Figure 1 shows the schematic view of the device structure of the Vertical MOSFET. While driving current of conventional SC-VMOS shown in Fig.2 (a) flows near only at the surface of the pillar, driving current of the proposed BC-VMOS shown in Fig.2 (b) flows throughout the pillar. By this BC-VMOS technique, potential profile in the pillar becomes more flat and relaxes the surface electric field inside the pillar (Esi) in comparison with SC-VMOS (Fig.2). Therefore, when the surface electron density (Qinv) is the same, the gate dielectric film's electric field (Eox) of BC-VMOS is more relaxed than the SC-VMOS according to Gauss's law ( $\varepsilon_{ox}E_{ox} = \varepsilon_{si}E_{si} + Q_{inv}$ ), where $\varepsilon_{ox}$ is the permittivity of gate dielectric film, such as $SiO_2$, $\varepsilon_{si}$ is the permittivity of the silicon.

By the above scheme, BC-VMOS can suppress the gate leakage due to FN or Direct tunneling phenomena and can keep excellent gate controllability and the same surface electron density (Qinv) in comparison with SC-VMOS. Therefore, it can be induced that the BC-VMOS gives excellent driving current performances with suppressed gate leakage.

## 3. Demonstration of Body Channel Type Vertical MOSFET Performance

In order to demonstrate the above mechanisms for BC-VMOS, two-dimensional device simulations of Vertical MOSFETs with the silicon pillar diameters (D) 50nm with gate length (Lg) 100nm is carried out including the gate-tunneling model, where data are obtained under 1μm width (W). A uniform p-type doping concentration of $1x10^{18}cm^{-3}$ is doped through the silicon pillar for SC-VMOS, and $4x10^{17}cm^{-3}$ is doped through the silicon pillar for BC-VMOS. The gate dielectric thickness (tox) is 2nm, which was chosen for the occurring large direct tunneling.

*A) Electric Field Suppression in Gate Dielectric Film*

Figure 3 and Fig.4 show electron density and potential profile in the body at direction X-X' in Fig.1 under the same Qinv ($=1x10^{18}cm^{-3}$). While the surface electron density of BC-VMOS is the same as SC-VMOS, BC-VMOS achieves an exponentially large electron density at the pillar center than SC-VMOS by the body channel type device design (Fig.3). Therefore, the potential of BC-VMOS becomes lower by 0.16eV than that of the SC-VMOS at pillar center (Fig.4). As a result, the surface electric field of BC-VMOS can be relaxed in comparison with SC-VMOS, while BC-VMOS has the same surface electron density as SC-VMOS.

By this BC-VMOS device design technique, BC-VMOS can suppress the applied voltage across the gate dielectric film by about 50% (Fig.5). Therefore, BC-VMOS suppresses the Eox by about 50%, which the gate dielectric film thickness is the same (Fig.6).

*B) Suppression of Gate Leakage Current*

Figure 7 shows the current-voltage characteristics of BC-VMOS in comparison with the SC-VMOS. The X-axis is Vgs – Vth in order to eliminate the effect of threshold voltage (Vth) difference between BC-VMOS and SC-VMOS. As shown in Fig.7, BC-VMOS can suppress the gate leakage current with the same ON driving current and OFF sub-threshold leakage in comparison with SC-VMOS. Figure 8 shows the gate leakage current of BC-VMOS normalized by SC-VMOS. Ratio of the gate leakage current BC-VMOS achieves low gate leakage current by 54 % in comparison with SC-VMOS.

Table I shows the performance improvements with BC-VMOS. Firstly, the Id/W with BC-VMOS is obtained almost the same as SC-VMOS. Secondly, the gate leakage current density (Jg) with BC-VMOS suppresses by 40%. The ratio of Id/W to Jg shows that BC-VMOS efficiently obtains the Id/W with suppressed Jg.

From the results above, the concept of BC-VMOS has been demonstrated.

## 4. Conclusions

In this paper, by our proposed Body Channel type Vertical MOSFET that changes its operation mode from conventional surface channel to body channel mode, the gate leakage current density can be suppressed by 54% than conventional surface channel type Vertical MOSFET under the conditions of keeping driving current and sub-threshold with constant gate dielectric film thickness. This

BC-VMOS is one of the candidates for future nano generation MOSFET with suppressed gate leakage current.

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**References**

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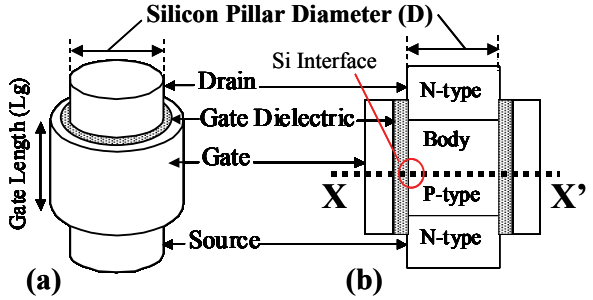


**Fig. 1:** Schematic view of device structure of Vertical MOSFET. (a) Bird's-eye view, (b) Cross section view.

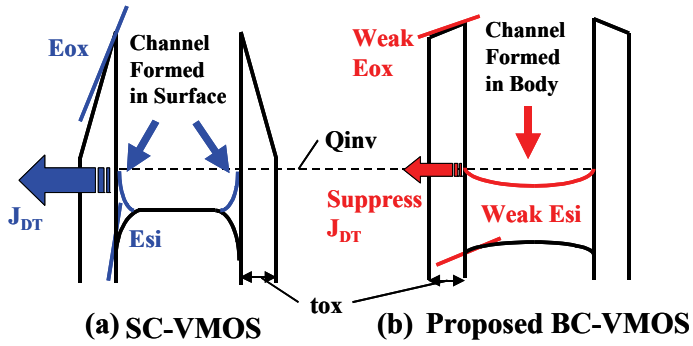


**Fig. 2:** Mechanism of suppression of gate leakage with Prop. BC-VMOS.

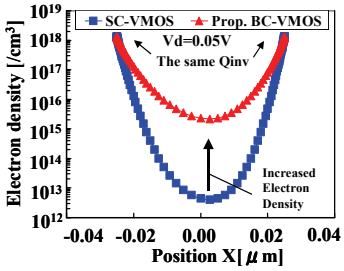


**Fig. 3:** Electron density in body at direction X-X' under the case of the same Qinv (=1x10$^{18}$cm$^{-3}$).

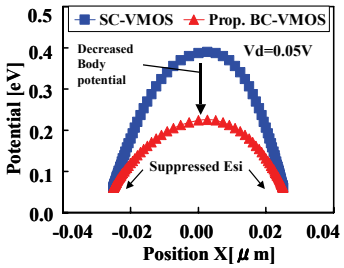


**Fig. 4:** Potential profile in body at direction X-X' under the case of the same Qinv (=1x10$^{18}$cm$^{-3}$).

**Table I:** Numerical comparison in driving and gate leakage current performances

| Bias point at Vgate=Vth+0.5V | Id/W Vd=0.05V [μA/μm] | Jg Vd=0.05V [A/cm²] | Ratio of Id/W to Jg Vd=0.05V |
|---|---|---|---|
| SC-VMOS | 2.31x10² | 1.14x10⁻² | 2.03x10⁴ |
| Prop.BC-VMOS | 2.52x10² | 6.85x10⁻³ | 3.68x10⁴ |
| Performance ratio of BC- to SC-VMOS | 1.09 | 0.60 | 1.81 |
| BC-VMOS performances to SC-VMOS | Almost the same | Suppress by 40% | Improve by 81% |

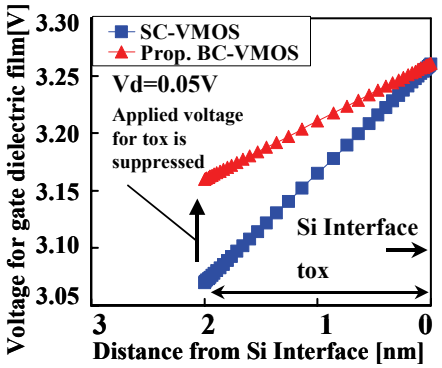


**Fig. 5:** Voltage for gate dielectric film under the case of the same Qinv (=1x10$^{18}$cm$^{-3}$).

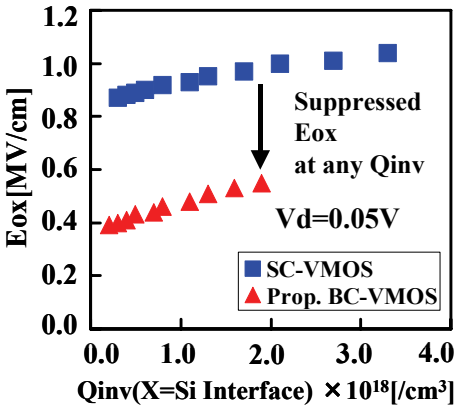


**Fig. 6:** Electric field at gate dielectric film as a function of Qinv.

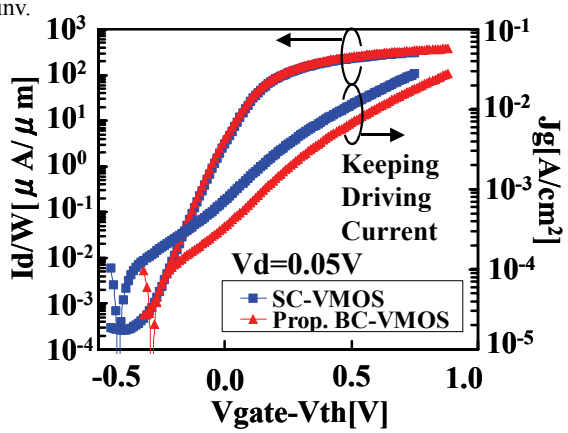


**Fig. 7:** Driving current characteristics with the gate leakage.

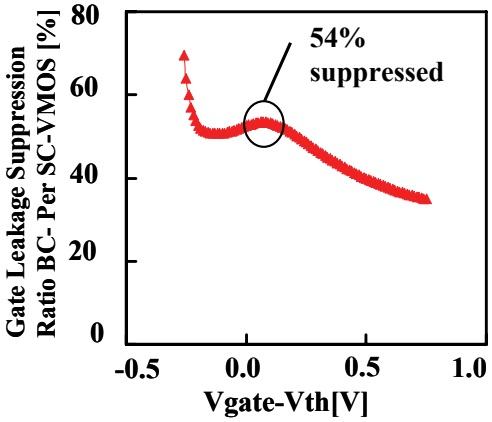


**Fig. 8:** Gate leakage current of BC-VMOS normalized by SC-VMOS.