Extended Abstracts of the 2011 International Conference on Solid State Devices and Materials, Nagoya, 2011, pp86-87

Saturation Behavior in the Generation of Interface Traps by Hot-Carrier Stress in Nanoscale MOSFETs

Ming Hu, Takuya Yamane and Toshiaki Tsuchiya

Shimane Univ.
1060 Nishikawatsu, Matsue, Shimane 690-8504, Japan
Phone & Fax: +81-852-32-6127 E-mail: tsuchiya@ecs.shimane-u.ac.jp

1. Introduction

As the dimensions of MOSFETs are scaled down to the nanometer regime, the number of interface traps in a nanoscale MOSFET becomes countable [1]. The characteristics of MOSFETs may be affected by the presence of very few or even individual interface traps. Interface traps can be generated in nanoscale MOSFETs during operation. Therefore it is important to characterize these newly generated interface traps and to study the impact that they have on the devices. In this paper, the process of interface trap generation due to hot carrier effects in nanoscale MOSFETs is evaluated by the charge pumping (CP) method. It is found (for the first time, to the best of our knowledge) that there is limit to the generation of interface traps by hot-carrier injection, and that the limit is determined by the energy of the hot carriers.

2. Experiment

All of the samples used in this study were poly-Si gate nMOSFETs that were carefully selected from the same wafer, with identical effective gate lengths and widths (L_{eff}=50 nm, W_{eff}=55 nm). The values of L_{eff} and W_{eff} were estimated from their transconductance. The gate-oxide thickness was 4 nm. The stress conditions are shown in Table I. The interface traps were evaluated using the charge pumping method [2]. The shape of the gate pulses that were used for charge pumping is shown in Fig. 1.

3. Results and Discussions

Hot-Carrier Stress and the Induced Device Degradation

The I_d-V_g characteristics before and after stress for all of the samples are shown in Fig. 2. The samples have been severely degraded due to extended stress time (up to 1×10^6 s). The threshold voltage shift (ΔV_{th}) during stress is shown in Fig. 3. The values of ΔV_{th} exhibit almost a sub-linear relationship with stress time t expressed as $\Delta V_{th}\sim t^n$, which is similar to the previous report [3]. The value of n from our results is about 0.3.

The initial values of I_{sub}/I_d are shown in Table I. I_{sub}/I_d for all samples increases during the stress, which indicates the generation of negative charges due to generated interface traps and/or trapped electrons within the oxide layer near the drain [4]. The dependence of threshold voltage upon drain voltage was measured in both normal mode and in "source-drain reversed mode" before and after stress. The V_{th} of stressed samples measured in reverse mode and the V_{th} measured before stress show similar dependences upon V_d, whereas the value of V_{th} of the stressed samples measured in normal mode shows a stronger dependence. This difference suggests that the generated negative charges that cause the shift in V_{th} shown in Fig. 3 are localized near the drain.

Saturation Behavior in the Generation of Interface Traps

The increase in ΔI_{cp} during the stress is shown in Fig. 4. All but sample #4 show a very clear saturation tendency. Sample #4 does not exhibit a clear saturation tendency because it failed at a comparatively early stage due to the highest value of I_{sub}/I_d, i.e., the strongest electric field.

The relationship between ΔI_{cp} at a stress time of 4000 s (before saturation) and I_{sub}/I_d, $I_{sub}\times I_{sub}/I_d$ are shown in Figs. 5 (a) and (b), respectively. It can be seen that ΔI_{cp} before saturation has no clear dependence on I_{sub}/I_d, but does have a linear dependence on $I_{sub}\times I_{sub}/I_d$, suggesting that the generation of interface traps before saturation is determined by both the number of hot carriers and their energies.

After longer stress, a saturation tendency does begin to appear for ΔI_{cp}. To better describe the saturation behavior of ΔI_{cp}, the conventional $\Delta I_{cp}\sim t^n$ relationship needs to be modified, as in the equation below,

$$\frac{1}{\Delta I_{cp}} = \frac{1}{\Delta I_{cpsat}} + \frac{1}{\alpha t^n} \quad , \qquad (1)$$

where ΔI_{cpsat} is the saturated value of ΔI_{cp} and α is used as a fitting parameter, though its physical meaning is currently not clearly understood. The lines in Fig. 4 are the calculated values of ΔI_{cp} using Eq. (1).

The relationship between the extrapolated values of ΔI_{cpsat} and I_{sub}/I_d is shown in Fig. 6, indicating that ΔI_{cpsat} increases with I_{sub}/I_d. Moreover, it should be noted that although Samples #3 and #5 have different stress conditions, they have similar I_{sub}/I_d, and ΔI_{cpsat} has almost identical values in each case. This can be explained by the mechanism of interface trap generation. The origins of interface traps, e.g., Si-H bonds [5], may be broken by the collisions with hot carriers. The higher the energy of the hot carriers, the stronger the bonds they can break. ΔI_{cpsat} is solely determined by the energy and is not related to the number of the hot carriers. On the other hand, ΔI_{cp} before saturation is determined by both the energy and the number of hot carriers, as shown in Fig.5 (b).

4. Conclusions

Saturation behavior in the generation of interface traps by hot carrier injection in MOSFETs is experimentally observed for the first time. The amount of the origins that are available to create interface traps within a MOSFET is limited by the energy of hot carriers.

Acknowledgement

This work was partially supported by the Semiconductor Technology Academic Research Center (STARC).

References

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Table I Stress Conditions

Sample	V_g (V)	V_d (V)	Initial I_{sub}/I_d ($\times 10^{-3}$)
#1	1.5	1.8	0.94
#2	1.5	2.0	2.91
#3	1.5	2.2	5.84
#4	1.0	2.2	7.73
#5	2.0	2.2	5.71

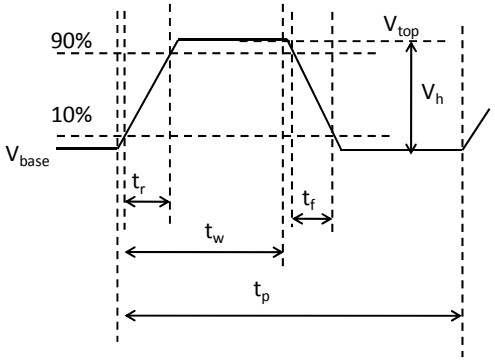


Fig. 1 Gate pulse of CP measurement. t_r=t_f=0.1 μs, t_w=2.0 μs, t_p=5.0 μs and V_h=2 V.

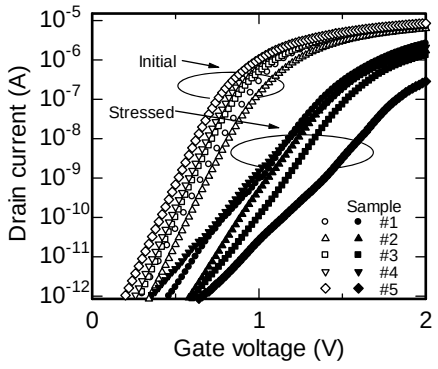


Fig. 2 I_d-V_g characteristics before and after stress.

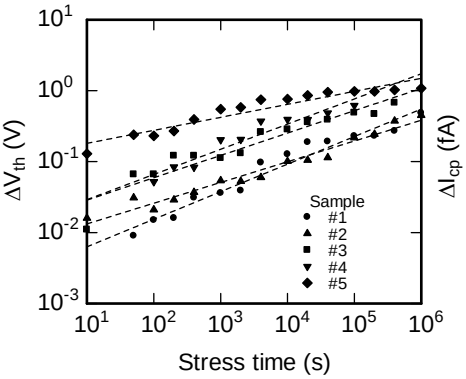


Fig. 3 Threshold voltage shift during stress.

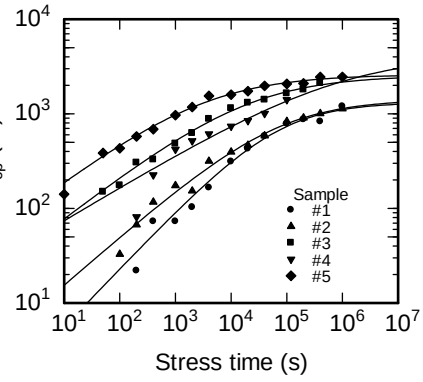
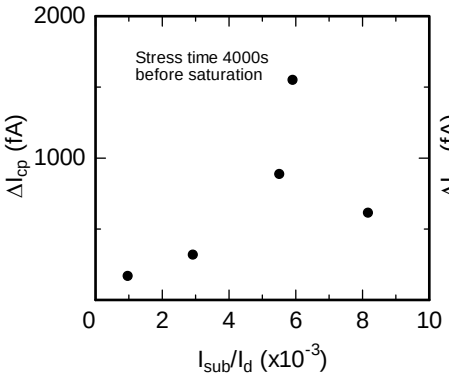
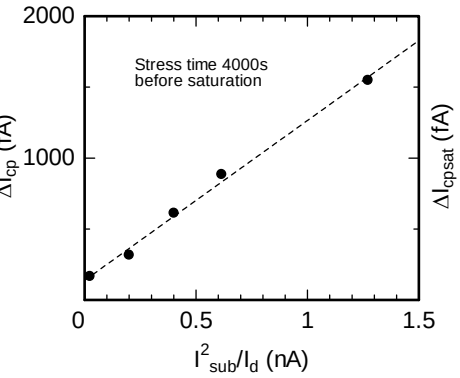


Fig. 4 ΔI_{cp} as a function of stress time.



(a)



(b)

Fig. 5 ΔI_{cp} before saturation as a function of (a) I_{sub}/I_d and (b) I^2_{sub}/I_d.

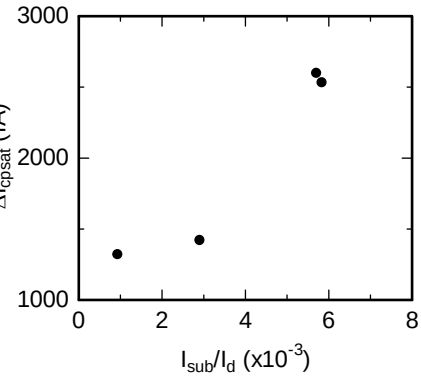


Fig. 6 ΔI_{cpsat} as a function of I_{sub}/I_d.