Impact of Poly Depletion on Accurate Evaluation of Self-Heating Effects in SOI MOSFETs with Four-point Gate Resistance Measurement Method

Nobuyasu Beppu1, Tsunaki Takahashi1, Teruyuki Ohashi1 and Ken Uchida1

Dept. of Physical Electronics1, Tokyo Institute of Technology, 2-12-1-S9-12, Ookayama, Meguro-ku, Tokyo 152-8552, Japan
Phone/Faxsimile: +81-3-5734-3854, E-mail: beppu@ssn.pe.titech.ac.jp

Abstract: This paper reports an accurate measurement method of self-heating effect (SHE) in SOI FETs. Although the method of using polysilicon gate as a temperature sensor was proposed more than 20 years ago, the accuracy of the technique has not yet been thoroughly checked. In this work, by measuring the gate resistance under various bias conditions, we found that the depletion of the polysilicon gate made a significant impact on the gate resistance, leading to a wrong estimation of the channel temperature. We propose a method to compensate for the poly depletion effect, resulting in an accurate evaluation of the channel temperature.

1. Introduction

FETs fabricated on SOI substrates are strong candidates for 16-nm technology node and beyond. However, since the thermal conductance (λ) of SiO2 is lower than Si by two orders of magnitude, the channel temperature (Tch) tends to be higher in SOI FETs than that in bulk FETs. Thus the self-heating effect (SHE) is more severe in SOI FETs. Since operation of FETs under high Tch reduces drain current (I) and decreases reliability of the devices, SHE is one of the most serious issues in SOI FETs. In order to cope with SHE, the accurate evaluation of Tch is indispensable. In this work, four-point gate resistance measurement [1, 2] is utilized to evaluate Tch (Fig. 1a). We found that the depletion of the polysilicon gate made a significant impact on the gate resistance (Fig. 1b), resulting in a wrong estimation of Tch. A method to compensate the poly depletion is proposed.

2. Experimental

Fig. 1a shows the device structure of measured devices. The polysilicon gate electrode takes four-terminal structure. The voltages applied to devices are measured by making the substrate bias as the reference. To measure polysilicon gate resistance without self-heating of the gate itself, the constant current bias of as low as 20μA is applied. The polysilicon gate resistance (RG) is evaluated as a function of temperature (Tch) of the hot chuck (Fig. 2). By using this RG-Tch relationship, Tch of devices under SHE is obtained from RG.

3. Results and Discussion

A. Four-point gate resistance measurement

Fig. 3 shows I and Tch as a function of the gate voltage (Vg) at the drain voltage (Vd) of 2 V. As is expected, Tch increases with an increase in I as well as power consumption (IVd). However, to our surprise, when Vg is as low as 0.5 V, a decrease in Tch with an increase in I is observed (Fig. 4). We consider that this is due to the stronger poly depletion at lower Vd. Fig. 5 shows RG as a function of Vg for various Vd. Fig. 6 shows Tch versus Vg characteristics obtained from Figs. 2 and 5. At Vg of 0.5 V, in the whole Vg range, Tch decrease is observed. When Vg is 1.0 V, Tch is decreased at Vg of greater than 3.0 V. These observations confirm that Tch decrease is observed when poly depletion is stronger.

In order to extract the effect of depletion on RG, RG is measured at Vg = Vd, where Vd is the source voltage. Since under the condition that Vg = Vd, no I flows in the channel and thus SHE is completely eliminated. Fig. 7 shows RG as a function of the gate voltage for various S/D voltages (Vg = Vd), demonstrating that RG increases as Vg increases even without SHE. In addition, as Vg increases (Vg decreases) RG decreases. These data clearly demonstrate that RG varies without SHE and that RG variation due to polysilicon gate depletion should be subtracted for the accurate evaluation of Tch.

B. Corrections for accurate gate resistance evaluation

However, evaluation of poly depletion in FETs under operation is not simple, because SHE and poly depletions are observed at the same time in realistic operation conditions. As an example of FET operation conditions, we consider a specific bias condition: Vg = 0 V and Vd = 2 V. In FETs under operation, channel potential (Vch) changes from Vg to Vd. The depletion is largest at the source edge (Vch = Vg = 0 V); it is smallest at the drain edge (Vch = Vd = 2 V). Therefore, two extreme bias conditions are considered to evaluate the poly depletion effect: one is Vg = Vd = 0 V (case A) and the other is Vg = Vd = 2 V (case B). Under FET operation condition, the polysilicon depletion condition is between the two extremes (Fig. 8). The change in RG in FETs under operation should be obtained by interpolating RG’s in case A and in case B. To find the interpolation formula, electron density in polysilicon gate is calculated using device simulator (Fig. 9). Since at higher electron density electron mobility is constant, RG is proportional to electron density. Fig. 9 shows the electron densities in polysilicon gate both in case A (red line) and case B (blue line). In addition, electron density in FETs under operation is also calculated (black line). As shown in Fig. 9, RG, in operation condition (black line) can be obtained by averaging RG’s in cases A and B.

To obtain the accurate Tch, it is necessary to measure RG’s in cases A and B. Then, the average of these two RG’s are subtracted from RG in FETs under operation. Fig. 10 shows the corrected Tch as a function of Vg for various Vd, indicating that Tch increases monotonically as input power increases. Fig. 11 shows the corrected Tch as a function of input power, demonstrating that the curves for various bias conditions overlapped. The obtained thermal resistance is 5.5-6.0 K/mW.

4. Conclusions

By measuring the gate resistance under various bias conditions, we found that the depletion of the polysilicon gate made a significant impact on the gate resistance, leading to a wrong estimation of the channel temperature. We propose a method to compensate for the poly depletion effect, resulting in an accurate evaluation of the channel temperature.

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Fig. 1: (a) Schematic of device structure. The polysilicon gate electrode takes four-terminal structure. (b) The polysilicon gate is depleted by gate bias, which makes the gate resistance high.

Fig. 2: Relationship between gate resistance ($R_G$), and channel temperature ($T_{ch}$).

Fig. 3: Drain current ($I_d$) and channel temperature ($T_{ch}$) increase as a function of gate voltage ($V_{gb}$) at drain voltage ($V_{db}$) of 2.0V.

Fig. 4: $I_d$ and $T_{ch}$ as a function of $V_{gb}$ at $V_{db} = 0.5V$. In spite of the larger power consumption at larger $V_{gb}$, $T_{ch}$ is lower.

Fig. 5: $R_G$ as a function of $V_{gb}$ for various $V_{db}$. Note that source voltage ($V_{sb}$) is equal to 0V.

Fig. 6: $T_{ch}$ as a function of $V_{gb}$ for various $V_{db}$ at $V_{sb} = 0$ V. $T_{ch}$ is calculated from Fig. 2 and Fig. 5 data.

Fig. 7: $R_G$ as a function of $V_{gb}$. The source voltage, $V_{sb}$, is the same as $V_{db}$. Thus, no current flows in the channel. The $R_G$ change is not caused by SHE but gate depletion.

Fig. 8: Polysilicon depletion conditions at $V_{gb} = 5.0V$. (a) $V_{db} = V_{sb} = 0V$; (b) $V_{db} = 2V$ and $V_{sb} = 0V$, (c) $V_{db} = V_{sb} = 2V$. This schematic is based on device simulation result.

Fig. 9: Simulated electron density in polysilicon gate. Operation condition (black line) is the average of the two extreme conditions (red line and blue line).

Fig. 10: Corrected $T_{ch}$ (solid lines) and non-corrected $T_{ch}$ (dashed lines) as a function of $V_{gb}$ at various $V_{db}$, $V_{sb} = 0$ V.

Fig. 11: Corrected $T_{ch}$ as a function of input power at various $V_{db}$. The corrected $T_{ch}$ curves (solid lines) are overlapped, whereas non-corrected curves do not merge.