Extended Abstracts of the 2011 International Conference on Solid State Devices and Materials, Nagoya, 2011, pp126-127

P-3-22L

Random Interface-Traps-Induced Characteristic Fluctuation in 16-nm High-κ/Metal Gate CMOS Device and Digital Circuit

Yung-Yueh Chiu[1], Yiming Li[1,2,*] and Hui-Wen Cheng[1]
[1]Institute of Communications Engineering, National Chiao Tung University, Hsinchu 300, Taiwan
[2]Deptartment of Electrical Engineering, National Chiao Tung University, Hsinchu 300, Taiwan
[*]Corresponding author. TEL: +886-3-5712121 ext. 52974; FAX: +886-3-5726639; and Email: ymli@faculty.nctu.edu.tw

Abstract

In this work, we for the first time study the DC and dynamic characteristic variability in 16-nm-gate high-κ/metal gate (HKMG) complementary metal-oxide-semiconductor (CMOS) devices and circuit induced by random interface traps (ITs) at Si/high-κ interface. Totally random devices with 2D ITs at Si/HfO_2 interface are incorporated into 3D device simulation. Random ITs' number, position and density on fluctuations of threshold voltage (V_{th}), on-/off-state current, gate capacitance, cutoff frequency, intrinsic gate delay, and noise margin (NM) of timings are explored. The results of this study indicate the random ITs induced fluctuation of NM is 20 mV which is smaller than 30 mV resulting from the random dopants. Note that the random position of ITs induces rather different fluctuations in DC/AC and timing in spite of the same number of ITs.

1. Introduction

HKMG technology has been known to a key way to suppress intrinsic parameter fluctuation for sub-22-nm CMOS generations [1-2]. However, the generation of random ITs at the interface of silicon and high-κ film introduces a new source of fluctuation for degradation of device characteristics. Recently, 1D and 2D ITs at the Si/high-κ interface have been proposed for sub-45nm CMOS devices [1,3]. Unfortunately, the study of 2D random ITs at the Si/high-κ interface has not been reported for 16-nm CMOS digital circuit yet. In this work, we study the random ITs induced DC/AC and timing characteristic fluctuations of 16-nm CMOS device and inverter circuit using an experimentally calibrated 3D device simulation. 2D ITs at the Si/HfO_2 interface are simultaneously considered in the 3D device simulation [1] which concurrently explore the effects of random number, position and density of ITs on device and circuit behaviors. The existence of random ITs results in high threshold voltage compared with nominal case. Not only DC base band characteristics but also gate capacitance (C_G) and transconductance (g_m) are altered. Consequently, cutoff frequency decrease and intrinsic gate delay increase as the number of random ITs increases. The noise margin fluctuation of CMOS inverter circuit is thus analyzed to show the performance degradation compared the random dopant induced fluctuation.

2. Simulation Methodology and Results Discussion

As shown in Fig. 1, the adopted DC characteristics of studied HKMG device follow ITRS roadmap for low operating power, which are experimentally quantified in our recent study [1-2]. Note that the magnitude of threshold voltage of nominal 16-nm CMOS devices is equal to 250 mV. The devices we examined are 16-nm planar MOSFETs (width: 16 nm) with amorphous-based TiN/HfO_2 gate stacks and an EOT of 0.8 nm, as shown in Fig. 1(a). For the simulation of 2D ITs fluctuation (ITF), we first generate 753 acceptor-like traps in a large 2D plane, as shown in Fig. 1(b), where the trap's concentration in the large plane is in the range of 1.5×10^{12} cm^{-2} based on an experimental characterization, and the total number of generated traps follows the Poisson distribution. Then, the statistically generated large plane is partitioned into many sub-planes, where the number of traps in sub-planes may vary from 1 to 8 and the average number is 4. The trap's energy on each sub-plane is assigned according to the distribution of trap's density [3,6-7]. We repeat this process until all sub-regions are assigned. Therefore, about two-hundred devices are generated for the 3D device simulation to calculate the ITF. The generated ITF devices are further implemented for 16-nm CMOS inverter circuit using coupled device-circuit simulation to estimated circuit level fluctuations, as shown in Fig. 1(c). Owing to lack of well-established compact models for 16-nm CMOS devices, a coupled device-circuit simulation is adopted, as shown in Fig. 1(d). This approach enables us to explore 16-nm CMOS digital circuit without compact models [1-2,4-5].

Figure 2(a) shows the I_D-V_G characteristic fluctuations of the ITs fluctuated 16-nm planar N-MOSFET, where the red solid line indicate the nominal case (i.e., the 3D device simulation without random ITs). The on-state currents (I_{on}), off-state currents (I_{off}), and threshold voltage are shown in Figs. 2(a)-(d), respectively. Each line and symbol shown in Figs. 2(a)-(d) indicate the DC characteristic for each device. The value of V_{th} is determined from a current criterion that the drain current larger than 10^{-7} (W/L) ampere. The V_{th} increases (and then the on-/off-state current decreases accordingly) as the number of ITs increases. The random ITs induced threshold voltage fluctuation ($\sigma V_{th,IT}$) is 26.3 mV which is smaller than the results of random dopant ($\sigma V_{th,RD}$ = 43 mV). In addition, the random position of ITs results in rater different fluctuations of characteristics in spite of the same number of traps, as marked in Fig. 2(d). Figs. 3(a) is the fluctuated gate capacitance (C_G-V_G) with respect to ITs, and the normalized C_G fluctuation is shown in Fig. 3(b). Not shown here, we also simulate the g_m as well as P-MOS device's characteristics. The g_m decreases as the number of ITs increases. Thus, the cutoff frequency and intrinsic gate delay of the studied N-MOS device are studied in Figs. 3(c) and 3(d), respectively, where the insets give the definition of these quantities. The intrinsic cutoff frequency of the studied device is decreased as the number of ITs is increased, and the intrinsic gate delay is increased as the number of ITs is increased. Fig. 4(a) shows the voltage transfer curves of the random ITs fluctuated 16-nm CMOS inverters. Two points on the voltage transfer curve determine the noise margins of the circuit. Figs. 4(b) and 4(c) show the noise margins for the logic "1" and "0," NM_H and NM_L, respectively, as a function of the ITs' number. Additionally, even the cases with the same number of ITs, there noise margin are still different due to ITs' random position effect. The NM_L increases as the number of ITs increases due to the increased V_{th} of the NMOS. For the NM_H , as numbers of ITs in the PMOS increase, the increased V_{th} of the device may decrease the V_{IH} of the voltage transfer curve and, thus, increase the NM_H. The fluctuations of NM_L (σNM_L = 20.1 mV) and NM_H (σNM_L = 20.3 mV) are similar, as shown in Fig. 4(d); however, the fluctuations of the noise margin low and high are also increased due to the more sources of fluctuation in the device channel surface. Note that the random ITs induced NMs are smaller than the random dopant induced σNM_L of 35mV and σNM_H of 30 mV [4,5], respectively.

3. Conclusions

In summary, the random 2D ITs induced fluctuations of DC/AC and timings were examined. The random ITs induced noise margin fluctuations of 16-nm CMOS inverter circuit, concurrently capturing the random ITs' number and position, were estimated; the random ITs induced σNM_L and σNM_H are associated with σV_{th} of P- and N-MOS devices, respectively. We are currently calibrating fabricated and measured 16-nm CMOS circuits.

4. Acknowledgement

This work was supported in part by National Science Council, Taiwan under Contracts NSC-99-2221-E-009-175, NSC-100-2221-E-009-018, and by TSMC, Hsinchu, Taiwan under a 2010-2011 grant.

References

[1] H.-W. Cheng et al., *in: IEDM Tech. Dig.*, 2010, pp. 379-382.
[2] Y. Li et al., *IEEE T. ED., vol. 57*, pp. 437-447, 2010.
[3] P. Andricciola et al., *IEDM*, pp. 341-344, 2009.
[4] Y. Li et al., *in: Proc. IEEE/ACM ICCAD* (2008) 278.
[5] Y. Li et al., *IEEE T. ED., vol. 56*, pp. 1588-1597, 2009.
[6] A. Appaswamy et al., *IEEE EDL., vol.* 31, pp. 387-389, 2010.
[7] A.T.M.G. Sarwar et al., *IEEE TENCON*, P0529, 5pp, 2009.

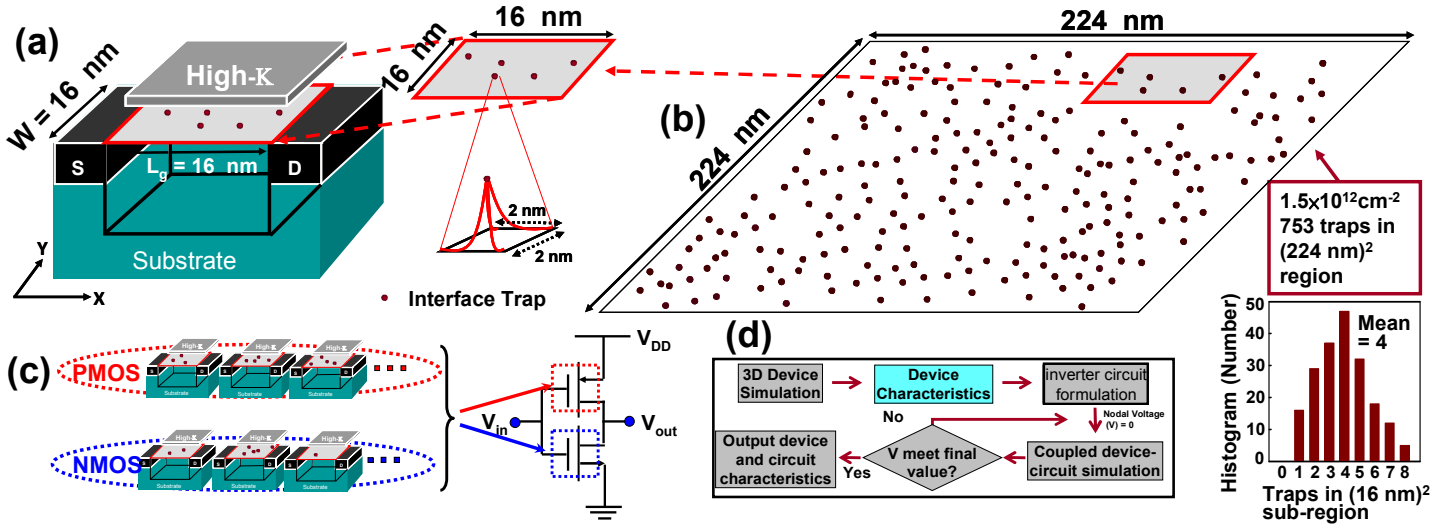

Fig. 1(a) The source of randomness (brown dots are interface traps) and simulation settings for fluctuations of random ITs. (b) We first generate 753 acceptor-like traps in a large plane, where the trap's concentration in the plane is around $1.5\text{x}10^{12}$ cm^{-2} and the total number of generated traps follows the Poisson distribution. The energy of each trap on the plane is assigned according to distribution of trap's density. Then the entire plane is partitioned into sub-planes (size: 16 nmx16 nm), where the number of traps in all sub-planes may vary from 1 to 8 and the average number is 4. (c) The generated ITF devices are implemented for 16-nm inverter circuit using coupled device-circuit simulation to estimated circuit level fluctuation. (d) The flow of coupled device-circuit simulation.

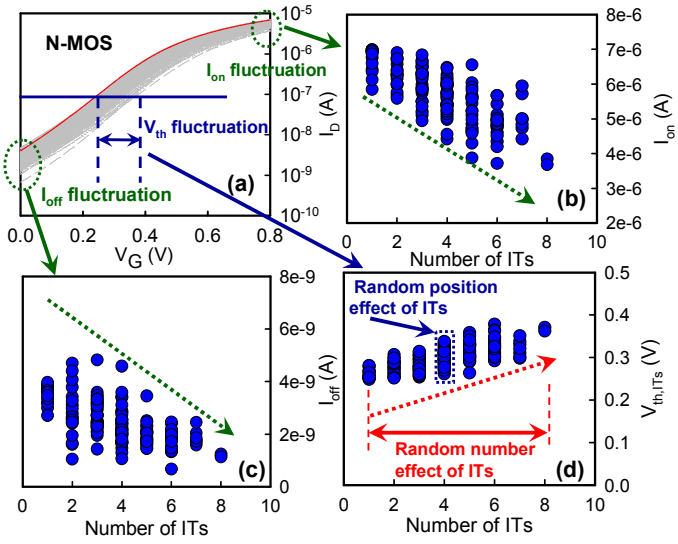

Fig. 2 The totally random ITs-induced DC characteristic fluctuations of (a) I_D-V_G characteristics, (b) and I_{on}, (c) I_{off}, and (d) V_{th} as a function of traps' number, where the red solid lines in I_D-V_G curves indicate the nominal case the dashed lines are fluctuated cases, the symbol line shows averaged result. The random position effect of ITs induces rather different fluctuation in spite of the same number of ITs marked in the inset of (d).

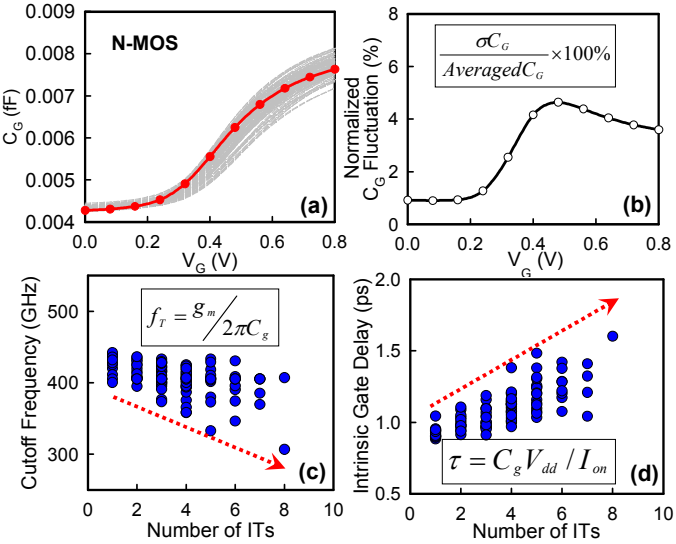

Fig. 3(a).The nominal (red), fluctuated (gray) capacitance-voltage characteristics, where the normalized C_G fluctuation is shown in (b). The intrinsic cutoff frequency and intrinsic gate delay are studied in Figs. 3(c) and 3(d), respectively, in which the insets give the definition of these characteristics.

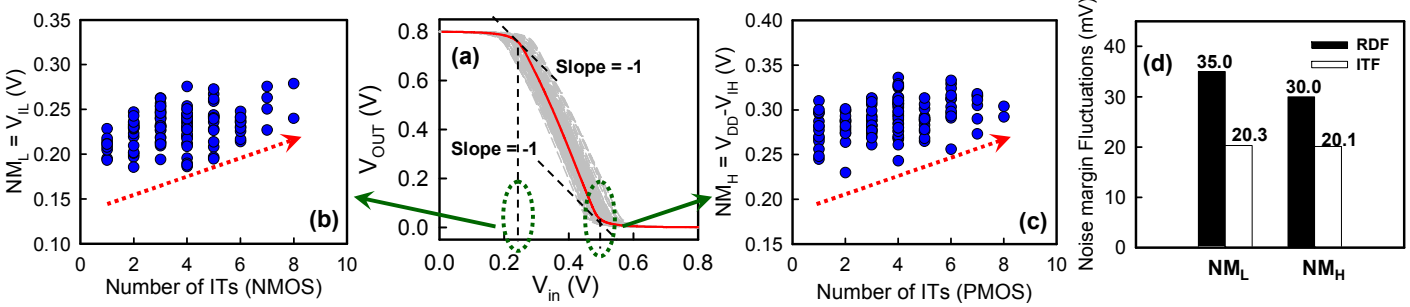

Fig. 4 (a) shows the voltage transfer curves for the 16-nm-gate CMOS inverters with ITs. The circled two points along V_{in} on the voltage transfer curve determine the noise margins of the inverter. Fig. 4(b) and (c) shows the noise margins for the logic "1" and "0" NM_H and NM_L , respectively, as a function of the ITs number. The noise margins of the inverter circuit increase as the ITs number increase. (d) The fluctuations of NM_L and NM_H with respect to different variation sources are shown in the insets of Fig. 4(d). The random dopants induced fluctuations of NMs dominate the results of random ITs.