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The Effect of La_2O_3 Capping Layer Thickness on Hot Carrier Degradation of *n*-MOSFETs with High-*k*/Metal Gate Stack

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1. Introduction

The continuous scaling down of gate oxide has induced the increases in gate tunneling current. To maintain low leakage current, high-*k*/metal gate stack is adopted. However, high-*k*/metal gate stack induces the threshold voltage V_{th} instability [1, 2], mobility degradation [3, 4], and reliability problems [5, 6]. The main challenge for successful integration of high-*k* oxide and metal gate is achieving low V_{th}. To obtain the appropriate V_{th}, the capping materials are developed. La_2O_3 capping layer is used for *n*-MOSFETs, and Al_2O_3 capping layer is used for *n*-MOSFETs. These capping layers control the effective work function of metal gate, and reduce the V_{th}. However, few reports have studied the effect of capping layer thickness on reliability of MOSFETs with high-*k*/metal gate stack. Since hot carrier effect is serious for short channel device, investigating the effect of La_2O_3 capping layer thickness on hot carrier degradation of *n*-MOSFETs with high-k/metal gate stack is important.

2. Experimental

The devices for the experiment were high-*k*/metal gate *n*-MOSFETs fabricated using 70 nm CMOS technology by Hynix Semiconductor Inc. All devices had the same channel length L of 75 nm and channel width W of 10 μm. The gate-first process was employed with TiN/HfSiO gate stack. La_2O_3 capping layers were deposited in different sequences and thicknesses either before or after HfSiO deposition to obtain bottom and top capping layer respectively. The thicknesses of La_2O_3 layers were 2, 5 or 10 Å, and the bottom layer of gate stack was SiO_2 interfacial layer of 10 Å.

The current-voltage (I-V) characteristics were measured by using HP 4156C semiconductor parameter analyzer, and the capacitance-voltage (C-V) characteristics were measured by using HP 4285A inductance-capacitance-resistance meter.

3. Results and Discussion

Fig. 1 shows the C-V characteristics of experimental devices measured at 100 kHz. The absolute value of flat band voltage V_{FB} increases as the thickness of La_2O_3 layer increases, so low V_{th} can be obtained from thick La_2O_3 layer. The position of La_2O_3 layer (i.e. either above or below HfSiO layer) does not influence V_{FB}.

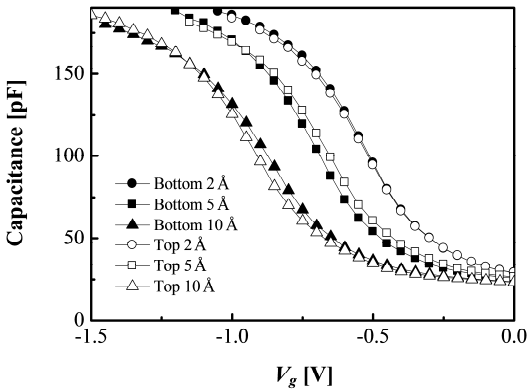

Fig. 1 The C-V characteristics of experimental *n*-MOSFETs.

Fig. 2 shows the characteristics of hot carrier degradation of experimental devices. The drain stress voltage $V_{d,str}$ is 3 V, and gate stress voltage $V_{g,str}$ is at peak substrate current I_{sub} which is drain-avalanche hot-carrier (DAHC) stress condition. The V_{th} degradation increases as the thickness of La_2O_3 layer increases irrespective of La_2O_3 layer position. This implies that there is a trade-off between V_{th} adjustment and reliability. Increasing the thickness of La_2O_3 layer to obtain low V_{th} causes the deterioration of device lifetime.

The V_{th} degradation is attributed to the generation of interface trap N_{it} and oxide trap N_{ot}. One way to measure the generation of N_{it} is checking the change in subthreshold slope ΔSS. The increase in interface trap density ΔD_{it} is obtained from [7, 8]

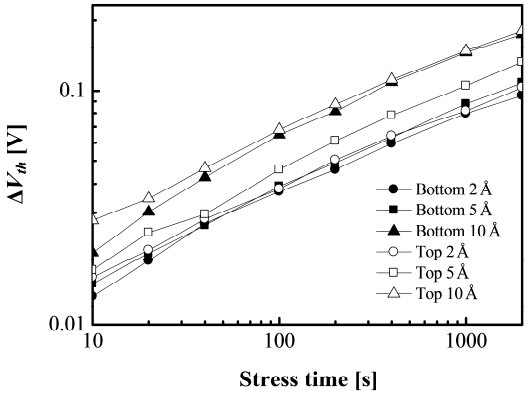

Fig. 2 The V_{th} degradation induced by hot carrier stress as a function of thickness and position of La_2O_3 layer.

$$\Delta SS = kT \cdot q \cdot \Delta D_{it} \cdot \ln(10) \qquad (1).$$

To investigate the effect of La_2O_3 layer thickness on ΔD_{it}, ΔSSs of experimental devices induced by hot carrier stress are measured. Fig. 3 shows I_d-V_g characteristics of 10 Å bottom capping layer MOSFET before and after hot carrier stress. A considerable ΔSS occurs after hot carrier stress of 2,000 s. The inset of Fig. 3 is ΔSSs with the change in thickness of La_2O_3 layer after hot carrier stress. There are little differences in *SS* degradation in case of top capping layer, but *SS* degradation increases as the thickness of bottom capping layer increases. Therefore, ΔD_{it} with the increases in stress time is intensified as the thickness of bottom capping layer increases.

From above results, 10 Å bottom capping layer MOSFET has more interface traps than 10 Å top capping layer MOSFET after hot carrier stress. However, the V_{th} degradations of two devices are almost the same. This is because the amount of N_{ot} generation after hot carrier stress is different each other.

Fig. 4 shows C-V characteristics of 10 Å top capping layer MOSFET, and there is a significant hysteresis of V_{FB}. From the inset of Fig. 4, V_{FB} hysteresis increases as the thickness of La_2O_3 layer increases. This hysteresis is attributed to N_{ot} [9, 10]. Top capping layer MOSFETs have more N_{ot} than bottom capping layer MOSFETs. Furthermore, the change in V_{FB} hysteresis with the change in thickness of top capping layer is much greater than that of bottom capping layer. This implies that thicker top capping layer MOSFET intensifies the generation of N_{ot} induced by hot carrier stress because MOSFET having many initial N_{ot} is more prone to degradation.

In summary, bottom capping layer influence the N_{it}, and top capping layer influence the N_{ot}. The increases in bottom capping layer thickness causes the increase in N_{it}, and the increases in top capping layer thickness causes the increases in N_{ot} during hot carrier stress. As a result, the thickness and position of La_2O_3 capping layer should be carefully chosen considering V_{th} adjustment and reliability.

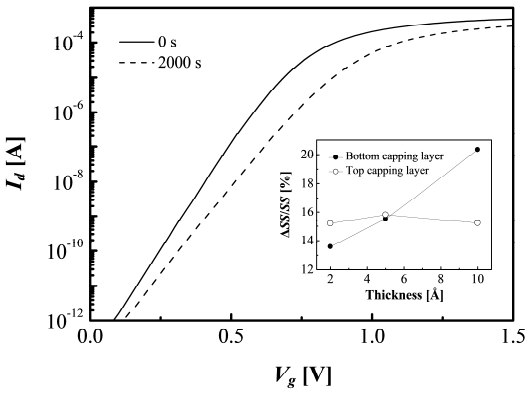

Fig. 3 The I_d-V_g characteristics of 10 Å bottom capping layer MOSFET before and after hot carrier stress. The inset shows ΔSS with the change in thickness of La_2O_3 layer after hot carrier stress of 2,000 s.

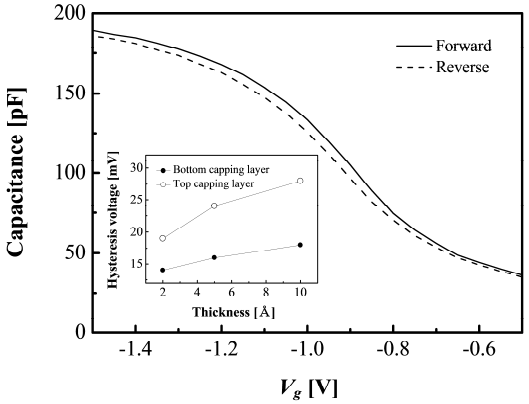

Fig. 4 The C-V characteristics of 10 Å top capping layer MOSFET. The inset shows V_{FB} hysteresis with the change in thickness of La_2O_3 layer.

4. Conclusions

The effect of La_2O_3 capping layer thickness on hot carrier degradation of *n*-MOSFETs with high-*k*/metal gate is investigated. Hot carrier degradation is monitored by measuring the threshold voltage V_{th} and subthreshold slope *SS*. As the thickness of La_2O_3 layer increases, the V_{th} degradation increases irrespective of La_2O_3 layer position. The generation of interface trap N_{it} is intensified during hot carrier stress as the thickness of bottom capping layer increases. On the other hand, the generation of oxide trap N_{ot} is intensified during hot carrier stress as the thickness of top capping layer increases.

Acknowledgements

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