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# Characterization of Oxide Traps in 28 nm pMOSFETs with Σ-Shaped SiGe-S/D by Utilizing Random Telegraph Noise (RTN)

Bo-Chin Wang[1*], San-Lein Wu[2], Shoou-Jinn Chang[1], Cheng-Tung Huang[3], and Osbert Cheng[3]

[1] Institute of Microelectronics and Department of Electrical Engineering, Advanced Optoelectronic Technology Center, Center for Micro/Nano Science and Technology, National Cheng Kung University, Tainan City 701, Taiwan

[2] Department of Electronic Engineering, Cheng Shiu University, Kaohsiung City 833, Taiwan

[3] Central R&D Division, United Microelectronics Corp. (UMC), Tainan City 744, Taiwan

Phone: +886-6-2757575 ext.62391 Fax: +886-6-2671854 *e-mail: q18981133@mail.ncku.edu.tw

## 1. Introduction

Channel strain engineering is currently recognized as an indispensable performance booster in producing next generation CMOS devices. In the case of pMOS devices, using embedded SiGe in the recessed source/drain region [1] can provide unaxial compressive strain in the channel. Moreover, Σ-shaped SiGe-S/D has closer proximity of embedded SiGe in source and drain region to the channel, which increased the channel stress than that of normal SiGe-shaped S/D, improves further pMOSFETs performance [2]. It is also reported that higher compressive stress on both side of the channel will degrade gate oxide quality near the source and drain edge of the dielectric layer [2], and need to be addressed on the behavior of oxide traps. The 1/*f* noise is a useful tool for evaluating the stress effect and monitoring the strain-induced interface properties. However, it is inadequate for small area devices (<1 μm$^2$) because there are existed larger noise level variation between the sample-to-sample [3]. In order to understand the trap property in small-area device, random telegraph noise (RTN) becomes much more important due to the capture and emission of single carrier at a gate dielectric trap [4]. In this paper, we explore the RTN in drain current of 28-nm node pMOSFETs with Σ-shaped SiGe-S/D, and investigate the physics-based properties of traps locations in the dielectric layer.

## 2. Device Structure and Experiment

The strained-Si pMOSFETs used in this letter were fabricated by a 28-nm technology CMOS process. Fig. 1 schematically shows the cross section of strained-Si pMOSFET with Σ-shaped SiGe S/D. The source/drain region is epitaxially grown B-doped SiGe film with 33% germanium concentration. For comparison, control devices without embedded SiGe S/D region have also been fabricated with the same process. The measured RTN was made by Waveform Generator / Fast Measurement Unit (WGFMU) measurement system based on Agilent B1500 Semiconductor Parameter Analyzer and measured in the drain current fluctuation of gate width (W) × gate length (L) = 0.25 ×0.1 μm$^2$.

## 3. Results and Discussion

Fig. 2 shows the drain current ($I_{DS}$) as a function of drain voltage ($V_{DS}$) for both pMOSFETs. It is found the $I_{DS}$ of pMOSFETs with Σ-shaped SiGe S/D improves approximately 56% compared with control counterparts at a fixed gate overdrive, $V_G$-$V_T$ = -0.8 V, and $V_{DS}$ = -1.0 V, which clearly indicates the Σ-shaped SiGe S/D process can efficiently induce compressive strain in the channel. In order to evaluate the effect of Σ-shaped SiGe S/D process on gate oxide/channel interface, the drain current fluctuation for both devices are shown in Fig. 3. A discrete switching of the current with time are found, which is controlled by carrier trapping/detrapping by a single trap in the vicinity of the channel of the devices [5]. The extracted mean capture time ($\tau_c$) and the mean emission time constant ($\tau_e$ ) versus gate overdrive ($V_G - V_T$) are presented in Fig. 4. The measured $\tau_c$ and $\tau_e$ for pMOSFETs with Σ-shaped SiGe S/D is observed to be lower than in the control counterparts, implying that the position of trap is closer to $SiO_2$/Si interface. This is because of the trap energy level near the channel valance band in pMOSFETs with Σ-shaped SiGe S/D due to the higher compressive strain in channel. Therefore, a hole can be captured or emission more easily.

Fig. 5 shows the dependence of $\tau_c/\tau_e$ on gate overdrive for both devices. The $\tau_c/\tau_e$ ratio is dominated by the difference between trap energy ($E_T$) and valence band ($E_v$). Smaller capture time than emission time observed in pMOSFETs with Σ-shaped SiGe S/D indicates that the trapping and detrapping events happen more frequently compared to the control device, confirming that the trap's location is closer to $SiO_2$/Si interface in Σ-shaped SiGe S/D device. From the data obtained for $\ln(\tau_e)$ dependence on gate voltage, the position of the trap into the oxide ($x_t$) are determined using Eq. (1) following [6]

$$\frac{\partial \ln(\tau_e)}{\partial V_{GS}} = \frac{q}{KT}\left(\frac{x_t}{t_{ox}}\right)\left[1 - \frac{KT}{q}\frac{G_m}{|I_{DS}|}\right] \qquad (1)$$

where $t_{ox}$ is the oxide thickness, K is Boltzmann constant and $\tau_e$ is emission time. Fig. 6 shows the trap position dependence on gate overdrive. The extracted $x_t$ are 0.4 and 1.0 nm for pMOSFETs with and without Σ-shaped SiGe S/D, respectively. Moreover, less $x_t$ dependence on gate voltage was found in the Σ-shaped SiGe S/D pMOSFETs. On the other hand, using information of vertical location of trap ($y_t$) and ratio of $\tau_c/\tau_e$ for forward bias and reverse bias, lateral location of trap could be extracted by Eq.(2) [7]

$$y_t = \frac{\left\{\frac{KT}{q}\left(\frac{t_{ox}}{x_t}\right)\ln\left[\frac{\ln(\tau_c/\tau_e)_f}{\ln(\tau_c/\tau_e)_r}\right] + V_{DS,r}\right\} \times L_{eff}}{V_{DS,f} + V_{DS,r}} \qquad (2)$$

Fig. 7 shows the results for both devices. Observed smaller distance between the trap and drain in Σ-shaped SiGe S/D device, as compared to control counterpart, confirming that higher compressive stain are responsible for the gate oxide quality degradation near the source and drain edge of the dielectric layer.

## 4. Conclusion

In this paper, we present the impact of compressive strain induced by Σ-shaped SiGe S/D on oxide trap properties. Through RTN measurement, we found that the trap position of pMOSFETs with Σ-shaped SiGe S/D has shorter distance from $Si/SiO_2$ interface and closer proximity to drain edge. This is because of the trap energy level near the channel valance band in pMOSFETs with Σ-shaped SiGe S/D due to the higher compressive strain in channel.


## Acknowledgements

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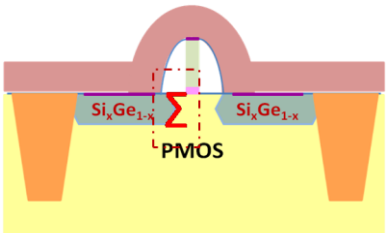


Fig. 1 Schematic of a pMOSFET for a planar embodiment with SiGe and Sigma-shaped recess in the source and drain.

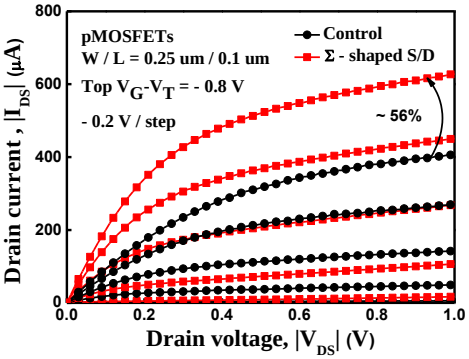


Fig. 2 $I_{DS}$-$V_{DS}$ characteristics of the pMOSFETs with the control and Σ - shaped S/D devices.

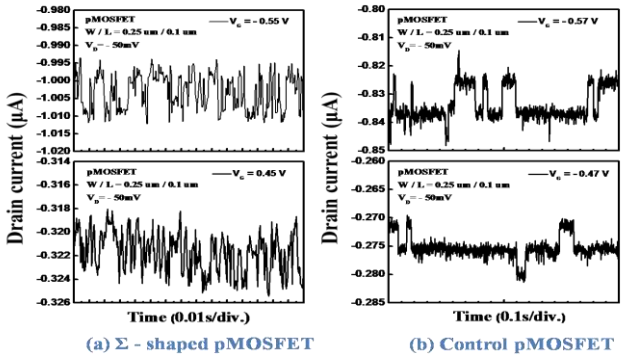


Fig. 3 Drain current waveform (a) Σ - shaped S/D (b) Control pMOSFETs..

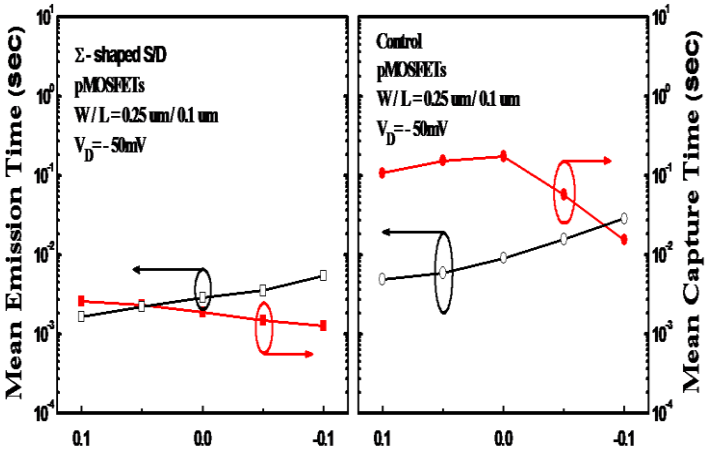


Fig. 4 Comparison of the capture time (filled ) and emission time (open ) for devices. (left)Σ - shaped S/D, (right) Control.

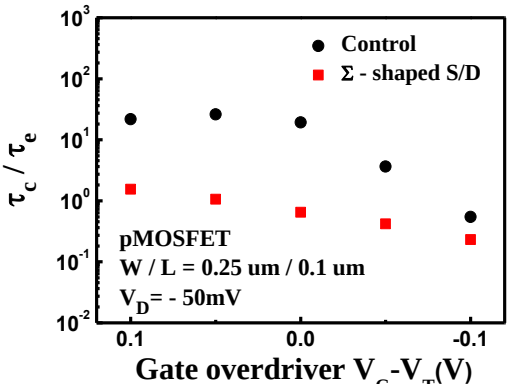


Fig. 5 Plot of $\tau_c$ / $\tau_e$ versus gate overdriver.

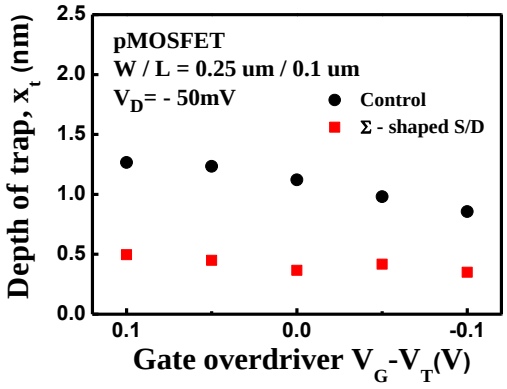


Fig. 6 Schematic of trap location in gate oxide for control and Σ - shaped S/D devices.

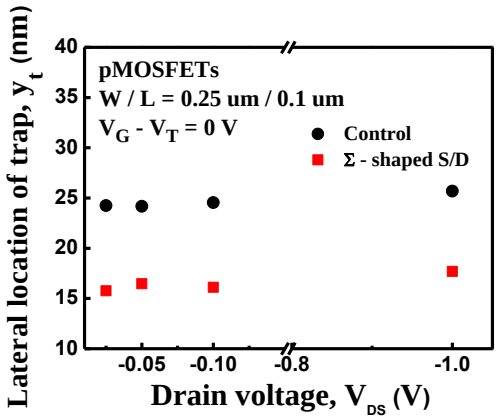


Fig. 7 Schematic of trap lateral position of traps by eq.(2).