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Hot-Carrier Effects on High-frequency Characteristics of RF LDMOS Transistors

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1. Introduction

LDMOS transistors have been widely used in RF power amplifier modules for high frequency range up to 3.8 GHz [1]. Because LDMOS used in power amplifier is operated at high drain voltage while carrying high current, it could be vulnerable to hot carrier injection and trapping. Therefore, the hot-carrier instability is one of the major reliability issues in an LDMOS, and has widely attracted attention in recent years [2][3]. However, the mechanisms of high-frequency parameter degradations have not been discussed in detail. In this paper, we present the experimental results of high-frequency characteristics of LDMOS transistors under hot-carrier stress.

2. Experiments

The n-channel LDMOS transistors were fabricated in a 0.5 μm CMOS-DMOS process with a gate oxide thickness of 135 Å and an effective channel length of 1.1 μm (Fig. 1). The off-state breakdown voltage is about 41 V. The devices under test have a multi-finger gate configuration featuring eight fingers with a total width of 80 μm. Constant bias hot-carrier stress was carried out by applying a gate voltage of 2.5 V and a drain voltage of 28V at room temperature. The applied gate voltage corresponds to the maximum body current. The S-parameters were measured on chip using an Agilent 8510 network analyzer from 100 MHz to 15 GHz.

3. Results and Discussion

Fig. 2 shows the hot-carrier effect on the dc characteristics of an LDMOS. The maximum value of transconductance (g_m) has about 3% degradation at drain voltage V_{DS}=0.1 V, probably due to the interface trap generation near the drain side of the channel. At V_{DS}=12 V, the drain current (I_D) and g_m degradations are not observed (<0.2%) before the quasi-saturation effect occurs. At high gate voltages, the device operation enters the quasi-saturation region, and the I_D and g_m reduces significantly after stress. From Fig. 3, we found the degradations of on resistance (R_{ON}) and saturation current ($I_{D,sat}$) are about 18% and 9%, respectively; they are higher than the degradation of linear g_m. It suggests that the stress-induced damage in the drift region is more serious than that in the channel region [3].

The gate voltage dependence of cutoff frequency (f_T) under hot-carrier stress is shown in Fig. 4. The maximum value of f_T is reduced by ~1.9% after 3 hr stress. It is much lower than the degradations of R_{ON} and $I_{D,sat}$, due to the different bias conditions. Besides, we found that although the g_m is unchanged by the stress at peak f_T, the f_T still has a slight degradation. This observation is different from that in MOSFET devices, where the g_m plays an important role in the f_T degradation [4]. Because the g_m is unchanged by the stress, the degradation of f_T may be attributed to the changes of gate capacitances.

The changes of gate-to-source capacitance (C_{gs}) and gate-to-drain capacitance (C_{gd}) under hot-carrier stress are shown in Fig. 5. Before quasi-saturation (V_{GS}<3 V), the C_{gs} increases with increasing stress time, while the C_{gd} reduces. The increase of C_{gs} under hot-carrier stress was also observed in MOSFET devices [5], and this phenomenon can be explained by the change of channel potential due to the appearing negative trap charges near the drain side of the channel. Owing to the existence of drift region, the decrease of C_{gd} after stress is different from the result in MOSFET devices [5], where the C_{gd} was nearly unchanged. In LDMOS, a large part of C_{gd} comes from the drift region. The stress-induced negative interface charges in the drift region lead to positive mirror charges in the silicon, thus reducing the effective N-well doping. As such the depletion layer width in the drift is increased and thus the C_{gd} is reduced. By plotting the degradations of f_T and total gate capacitance (C_{gg}=C_{gs}+C_{gd}) as functions of stress time (Fig. 6), we found that the changes of f_T and C_{gg} are similar. It confirms that the f_T degradation is dominated by the change of gate capacitance.

Fig. 7 shows the degradation of maximum oscillation frequency (f_{max}) under hot-carrier stress. The maximum value of the f_{max} is nearly unchanged with stress time (<0.5%). Because the gate resistance is not affected by the hot carriers, we only consider the effects of f_T and C_{gd} on the f_{max}. After 3 hr stress, the f_T and C_{gd} are reduced by 1.9% and 2.0%, respectively, at the bias condition of V_{GS}=2.6 V and V_{DS}=12 V. Similar degradation in f_T and C_{gd} leads to a slight change of the f_{max}. At high gate voltages, large f_{max} degradations are observed due to the obvious f_T reduction and C_{gd} enhancement.

4. Conclusions

After hot-carrier stress, the f_T is reduced, while the f_{max} is almost kept at the same value when the device operates before the quasi-saturation effect occurs. This observation

can be explained by the changes of C_{gs} and C_{gd}, owing to the generated trap charges in the channel and drift regions, respectively. In addition, the f_T and f_{max} degradations are less than that in R_{ON} and $I_{D,sat}$, indicating the hot-carrier instability is less serious when the LDMOS is used in RF power amplifiers, as compared to that used in the power switching circuits.

Acknowledgements

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References

[1] F. van Rijs, IEEE Radio and Wireless Symp., (2008) 69.

[2] P. Moens et al., IEEE Trans. Electron Devices, **51** (2004) 1704.

[3] P. Moens et al., Proc. IRPS, (2007) 492.

[4] S. Y. Huang et al., IEEE SiRF Digest, (2006) 81.

[5] Y. T. Yew et al., IEEE Electron Device Letters, **12** (1991) 366.

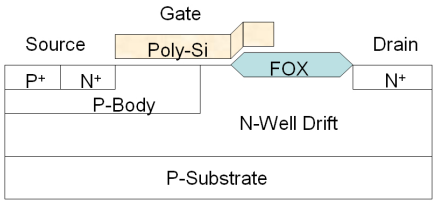

Fig. 1 Schematic cross section of an LDMOS transistor.

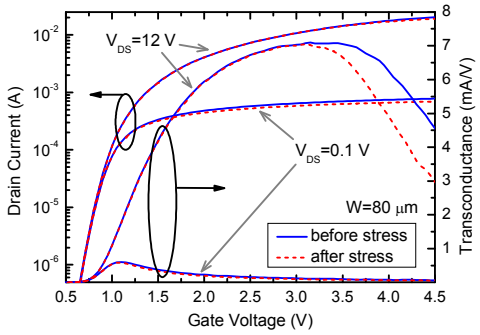

Fig. 2 Measured transfer characteristics of an LDMOS before and after 3 hr hot-carrier stress.

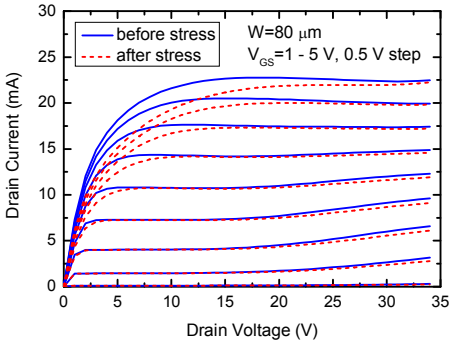

Fig. 3 Measured output characteristics of an LDMOS before and after 3 hr hot-carrier stress.

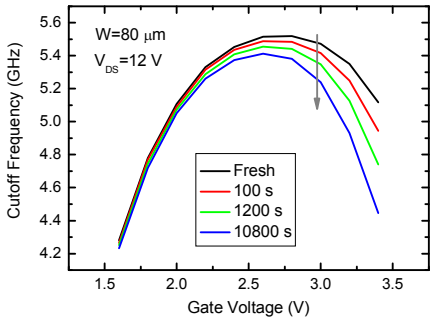

Fig. 4 Measured cutoff frequency as a function of gate voltage for an LDMOS under hot-carrier stress.

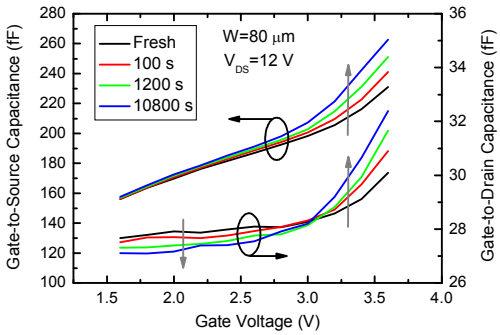

Fig. 5 Extracted gate capacitances as a function of gate voltage for an LDMOS under hot-carrier stress.

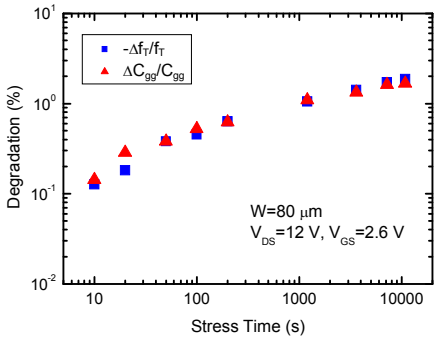

Fig. 6 Degradations of cutoff frequency and total gate capacitance under hot-carrier stress.

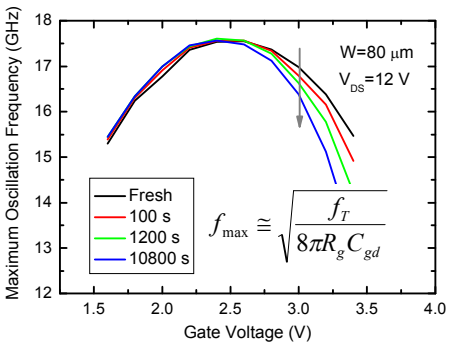

Fig. 7 Measured maximum oscillation frequency as a function of gate voltage for an LDMOS under hot-carrier stress.