Impact of OFF-state Degradation under Dynamic Stress on Reliability of Nanoscale n-Channel Metal-Oxide-Semiconductor Field-Effect Transistors at Elevated Temperature

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1. Introduction

In a CMOS inverter operating at a dc supply voltage $V_{dd}$, the nMOSFET subjects to a gate voltage $V_g = 0$ V and drain voltage $V_d = V_{dd}$ during the OFF-state period, and to $V_g = V_{dd}$ and $V_d = 0$ V during the ON-state period. Because the inverter is operated in the dynamic condition alternating between the OFF and ON-states, the dynamic stress degradation should be investigated carefully. To date, previous studies for the dynamic stress of nMOSFETs focused on the degradations which can be induced by drain avalanche hot carrier (DAHC) or channel hot carrier (CHC) during short rising/falling time. For scaled nMOSFET, it has been reported that the OFF-state drain current $I_{off}$ flowing from source to drain by drain induced barrier lowering (DIBL) can induce impact ionization and cause the OFF-state hot carrier degradation. However, the effect of OFF-state degradation under the dynamic stress has not been discussed yet. This work focuses on the impact of OFF-state degradation under the dynamic condition on the reliability of nanoscale nMOSFETs at high temperature $T$. First, shifts of threshold voltage $V_{th}$ by the dynamic and various static stresses at high $T$ were compared. Second, $T$ dependency of degradations by the dynamic and OFF-state stresses was examined. Then, the behaviors of $V_{th}$ and $I_{off}$ when switching from the OFF- to ON-state were described to explain the detailed degradation mechanism of the dynamic stress. Our new observations indicate that the OFF-state degradation can influence significantly the reliability of scaled CMOS inverter circuits.

2. Devices and Experiments

The devices for the experiment were n+ poly gate nMOSFETs with gate length and width of 0.078 μm and 10 μm, respectively. The gate oxide thickness (2.2 nm) was fabricated using decoupled plasma nitridation (DPN). The various stress modes under the dynamic condition in an inverter are shown in Fig. 1 (ON-state, CHC/DAHC during short rising/falling time, and OFF-state). A dynamic stress with frequency $f$ of 100 kHz (duty cycle of 50%) and static stresses at $V_{dd} = 2.8$ V was applied to the nMOSFETs at temperatures $T = 125$ °C, while the source and substrate were grounded. The $V_{th}$ was defined as the $V_g$ which resulted in $I_d = 2$ μA/μm.

3. Results and Discussion

The shifts of $V_{th}$ by the various stress modes were measured at $T = 125$ °C, as shown in Fig. 2. The worst-case degradation of $ΔV_{th}$ was observed in the dynamic stress. The $ΔV_{th}$ was not changed by the CHC and ON-state stresses, but it was increased by the OFF-state stress. This implies that the OFF-state degradation is related to that of the dynamic stress although it was much lower than that of the dynamic stress (The $ΔV_{th}$ for 3000s of OFF-state stress was ~74% lower than that of the dynamic stress). To understand the degradation characteristics of dynamic stress, the devices with different gate length $L_g$’s were subjected to the dynamic stress for 3000s, as shown in Fig. 3. The dynamic stress shifted $ΔV_{th}$ slightly for the long channel devices but significantly for the short channel ones. The inset of Fig. 3 shows the shift of $I_{off}$-$V_g$ curves before and after the dynamic stress for $L_g = 0.078$ μm. The dynamic stress increased the sub-threshold slope $SS = \partial V_g/\partial \log(I_d)$ and decreased the sub-threshold current $I_{sub,th}$, meaning that the interface trap $N_i$ and negative oxide charge $Q_{ox}$ were generated. These behaviors appear to be similar to the typical hot carrier degradation. In contrast, the $ΔV_{th}$ at $T = 25$ or 75 °C was lower than that at $T = 125$ °C, which is similar to the trend of typical DAHC degradation. In contrast, the $ΔV_{th}$ at $T = 25$ or 75 °C was lower than that at $T = 125$ °C. This behavior agrees with that of the OFF-state degradation, as shown in the inset of Fig. 4. The experimental results shown in Fig. 2-4 indicate that the OFF-state hot carrier degradation is the main cause of the dynamic stress degradation at $T = 125$ °C, which can be explained from the increase in DIBL-induced $I_{off}$ because the intrinsic carrier density $n_i$ exponentially increases with the $T$. To further investigate the degradation mechanism of the dynamic stress at high $T$, the $ΔV_{th}$ and $ΔL_{off}$ (measured at $V_g = 0$ V, $V_d = 2$ V) versus the stress time alternating between the OFF and ON-states were measured at $T = 125$ °C, as shown in Fig. 5. The OFF-state stress increased $ΔV_{th}$ slowly, but it also increased $ΔL_{off}$ despite the increase in $ΔV_{th}$. This indicates that the $N_i$ and positive $Q_{ox}$ are generated due to the OFF-state stress, which the predominance of $N_i$ explains the increase in $V_{th}$. The subsequent ON-state increased $ΔV_{th}$ abruptly and decreased $ΔL_{off}$ significantly. This behavior originated from the OFF-state stress because the ON-state stress did not shift $ΔV_{th}$ (see Fig. 2). An increase in $V_{th}$ is possible when the $N_i$ or negative $Q_{ox}$ are generated. The
behavior of $N_{it}$ was monitored by the shift of DCIV current $I_{DCIV}$. In Fig. 6, the $\Delta I_{DCIV}$ was increased by the OFF-state stress, but it was not changed by the ON-state, indicating that the $N_{it}$ is not the source of the subsequent ON-state degradation. This result is consistent with the behavior of $\Delta SS$ in the inset of Fig. 6. Accordingly, the observed shifts of $\Delta V_{th}$ and $\Delta I_{off}$ are mainly attributed to the negative $Q_{ox}$. The bias condition for ON-state allows electron injection into the gate oxide. Therefore, it is obvious that the hot holes increased by high $T$ during the OFF-state generates neutral electron traps by breaking Si-O bond close to the Si interface and the subsequent ON-state fills the electron traps, which caused the abrupt shifts of $\Delta V_{th}$ and $\Delta I_{off}$. In addition, the positive $Q_{ox}$ generated by the OFF-state stress can act as an electron trap during the ON-state because it can be neutralized by the electron injection, which caused the slow shifts of $\Delta V_{th}$ and $\Delta I_{off}$. When the second OFF-stress was applied, the electron traps near the Si interface returned to the unoccupied state at the initial, which resulted in the abrupt decrease in $\Delta V_{th}$ and increase in $\Delta I_{off}$. The electron traps located far from the interface might have not returned to the original state. This made $\Delta V_{th}$ and $\Delta I_{off}$ at the initial period of second OFF-state not equal to those at 3000s. From these experimental results, we can conclude that three defects ($N_{it}$, positive $Q_{ox}$, and neutral electron trap) are generated during the OFF-state period and their effects during the ON-state are the main cause of the dynamic stress degradation at high $T$. This new observations indicate that the OFF-state degradation should be taken seriously when evaluating reliability of scaled CMOS inverter circuits.

4. Conclusions

The impact of the dynamic condition of a CMOS inverter on reliability of nanoscale nMOSFET at high $T$ was investigated. Significant dynamic stress degradation was observed at high $T$. The experimental results indicate that three types of defects are generated during the OFF-state period and they are filled by the electron injection during the ON-state period, thus resulting in the significant device degradation. Our results suggest that the OFF-state degradation should be taken seriously when evaluating reliability of scaled CMOS inverter circuits.

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References