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Pushing Scaling Limit Due to Short Channel Effects and Channel Boosting Leakage from 13nm to 8nm with SOI NAND Flash Memory Cells

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1. Introduction

There is a strong demand for continuous scaling in floating-gate (FG) type NAND flash memories below 20nm generation. However, serious program disturb errors due to the interferences from neighboring cells [1-4] become prominent. On the other hand, channel engineering and its scaling limitation in NAND flash memory cells are also concerns [5, 6]. Due to the large EOT (16~20nm) in NAND cells, short channel effect (SCE) is degraded in scaled generations. As a result, DIBL induced program disturb has been reported [7]. Also, operation margins may decrease in MLC technologies since large S-factor worsens on/off current ratio [8]. However, suppressing SCE by high channel doping concentration leads to junction leakage during program-inhibit in bulk NAND flash memories [5].

A thin body, thin BOX fully depleted SOI NAND flash memory is one of the candidates for the future scaled NAND flash memory for the excellent SCE controllability [6, 8]. Moreover, the drawbacks of thin body SOI transistors such as high parasitic resistance, low V_{TH} controllability by channel doping and V_{TH} increase by quantum confinement are less critical in the NAND flash memory than in logic device because the NAND flash memory does not require high cell current during the read and precise initial V_{TH} control (V_{TH} is controlled by the amount of electrons in the FG). In this paper, the scaling trends of bulk and SOI NAND cells are newly investigated in terms of SCE and leakage during channel boosting from 20nm to below 10nm generation using 3D-device simulation. It is found that the SOI NAND pushes the scaling limit of the SCE and channel boosting leakage from 13nm to 8nm generation.

2. Device Design and Simulated Device Structure

Fig. 1 shows the program operation of a NAND flash memory. In a program-inhibit bit-line, channel voltage of the NAND string is boosted up to more than 8V to avoid V_{PGM} cell disturb. Thus, the junctions of the NAND cells must withstand high voltage stress. Otherwise, junction leakage occurs and program-inhibit fails because the channel voltage does not sufficiently increase. Hence, channel doping concentration cannot be increased in a bulk NAND cell for suppressing SCE. In SOI NAND flash cell, thinner BOX has better SCE characteristics while too thin BOX may cause BOX leakage during channel boosting. If there is no BOX leakage, channel leakage is greatly reduced because the junction area is very small.

Considering above, the device design in this work is discussed. Figs. 2(a) and 2(b) show the device structure of the bulk and SOI NAND flash memory cells at 15nm generation used in this simulation. Bulk source/drain junction depth X_j and SOI thickness T_{SOI} are fixed to 6nm. Punch-through stopper (PTS) layer, where the doping concentration is higher than the other channel region, is added to the bulk cell. T_S (distance between PTS layer and source/drain junction) is changed to control the SCE. Although SCE is better in smaller T_S, the junction leakage increases. For the SOI NAND cell, T_{BOX} (BOX thickness) is varied.

3. SCE and Channel Boost Characteristics of Bulk and SOI NAND Flash Memory Cells

Channel leakage during channel boosting of the bulk and SOI NAND cells having the same SCE characteristics are compared. Junction electric field ($E_{junction}$) and BOX electric field (E_{BOX}) are evaluated for the channel leakage. Fig. 3 shows the V_{TH} roll-off (ΔV_{TH} is the V_{TH} difference from the V_{TH} at L_g=20nm) of bulk and SOI NAND cells at 15nm generation. T_S and T_{BOX} are chosen to meet the same roll-off characteristics in both bulk and SOI technologies. Figs. 4(a) and 4(b) show the S-factor and DIBL versus L_g in 15nm generation. Although the bulk and SOI NAND cells have the same V_{TH} roll-off characteristics in Fig. 3, S-factor and DIBL in the SOI NAND cell are better.

Figs. 5(a) and 5(b) show the potential profile during the channel boosting simulation at 11nm generation for bulk and SOI NAND cells, respectively. SCE in both bulk and SOI NAND cells are made the same as the case in 15nm generation. Source and drain voltages are set to 8V. In the bulk NAND cell (Fig. 5(a)), $E_{junction}$ is found to be higher than 1MV/cm, which is the critical value for the junction leakage. Thus, channel boost in the bulk cell fails at 11nm generation. On the other hand, E_{BOX} in the SOI NAND cell is found to be below 10MV/cm where FN tunneling starts to occur. Note that BOX is made of thermal oxide and its quality is higher than that of the oxide (typically TEOS) filled between the FGs and CGs. Therefore, no BOX leakage occurs even at 11nm generation in the SOI cell. Figs. 6(a) and 6(b) are the $E_{junction}$ and S-factor as a function of T_S in bulk technology, respectively, at 13nm and 11nm generation. Although $E_{junction}$ is below 1MV/cm except for T_S=0nm at 13nm generation, $E_{junction}$ exceeds 1MV/cm at 11nm generation for all T_S. S-factor for 11nm generation is also worse than 13nm generation. E_{BOX} and S-factor in the SOI NAND cell as a function of T_{BOX} are shown in Figs. 7(a) and 7(b). E_{BOX} is still below 10MV/cm at 11nm generation for all T_{BOX}. S-factor can be also slightly improved by reducing T_{BOX}.

The scaling trends for the $E_{junction}$/E_{BOX} and S-factor of the bulk and SOI NAND cells are shown in Figs. 8 and 9. From Fig. 8, the scaling limit of the bulk NAND cell from the perspective of the junction leakage failure is 13nm generation. In the SOI NAND cell, the scaling limit decreases to 8nm. Fig. 10 shows the trends of g_{m_max} in bulk and SOI technologies. The g_m of SOI NAND cell is larger than the bulk NAND cell. From these results, a SOI NAND cell can reduce the channel boosting leakage with good SCE characteristics.

4. Conclusion

The scaling trends and limits of the bulk and SOI NAND flash memories are investigated in terms of SCE and channel boosting leakage from 20nm to below 10nm generation using 3D-device simulation. In the bulk NAND cell, 13nm generation is the scaling limit for realizing both channel boosting during program-inhibit and SCE suppression. The SOI NAND cell scaling limit is decreased to 8nm generation.

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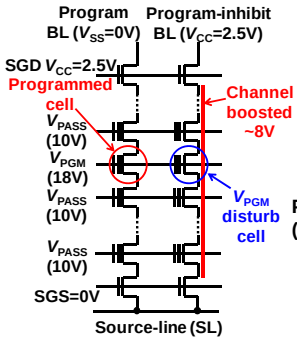

Fig. 1 Schematic of the program operation in a NAND flash memory. Channel voltage is boosted in program-inhibit bit-line and high drain-substrate voltage is applied to the cells

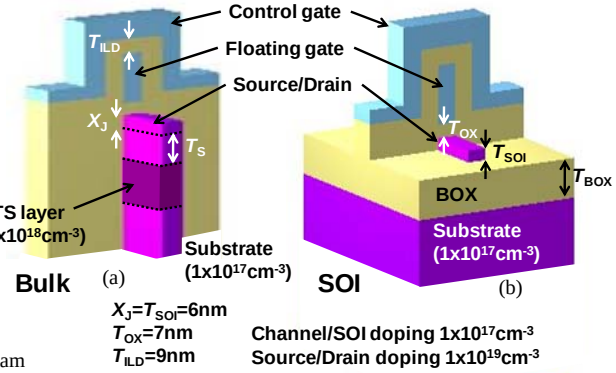

Fig. 2 Device structure of (a) bulk and (b) SOI NAND flash memory cells at 15nm generation for the 3D-simulation in this work. Punch-through stopper (PTS) layer is used in the bulk NAND cell to suppress SCE.

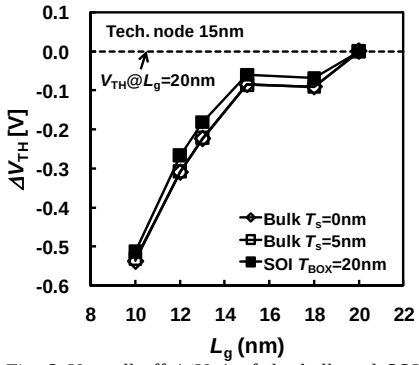

Fig. 3 V_{TH} roll-off (ΔV_{TH}) of the bulk and SOI NAND cells at 15nm generation. Roll-off characteristics in both bulk and SOI NAND cells are designed same.

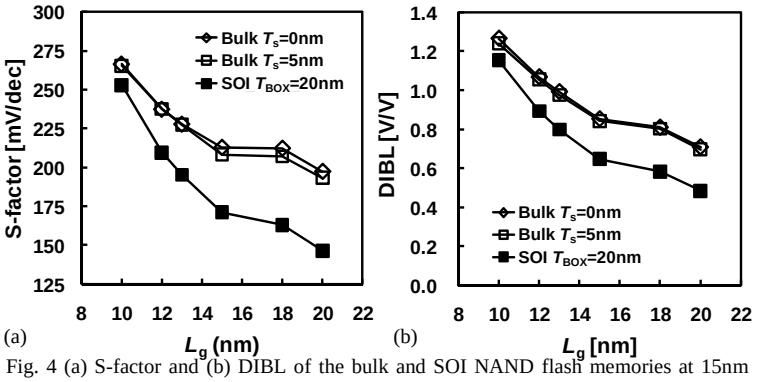

Fig. 4 (a) S-factor and (b) DIBL of the bulk and SOI NAND flash memories at 15nm generation.

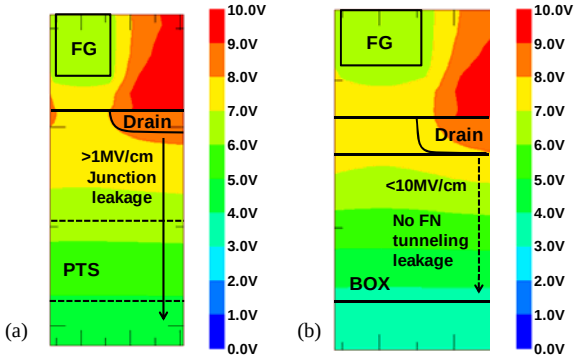

Fig. 5 Potential profile of the (a) bulk and (b) SOI NAND flash memory cells at 11nm generation during channel boosting.

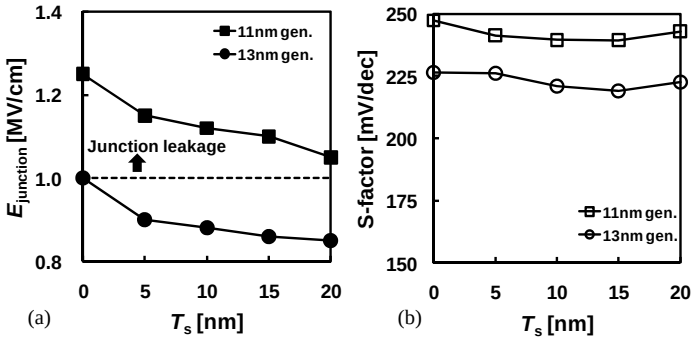

Fig. 6 (a) Electric field at the drain-substrate junction $E_{junction}$ in a bulk NAND cell as a function of T_s (distance between PTS layer and drain junction). (b) S-factor as a function of T_s. At 11nm generation, the bulk NAND cell fails to boost the channel by the junction leakage due to the high $E_{junction}$.

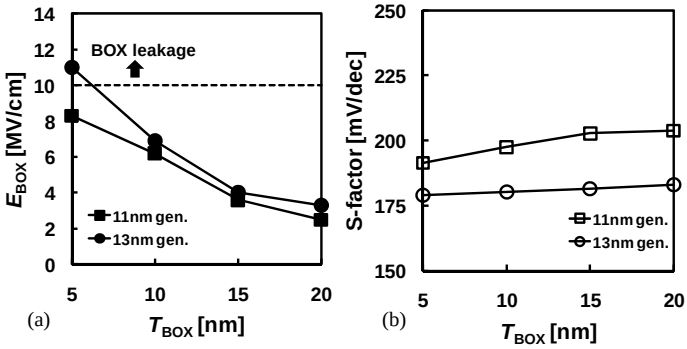

Fig. 7 (a) Electric field of the BOX layer at the drain E_{BOX} in a SOI NAND cell as a function of T_{BOX} (BOX layer thickness). (b) S-factor as a function of T_{BOX}. Above T_{BOX}=5nm, the SOI NAND cell satisfies both small E_{BOX} and S-factor even at 11nm generation.

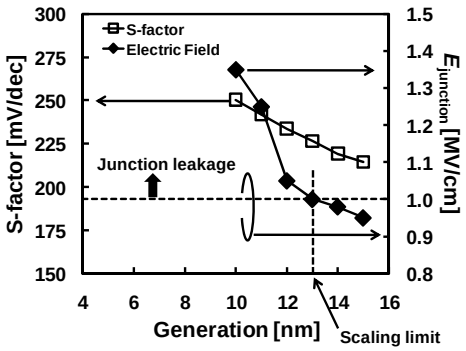

Fig. 8 Scaling trend of the S-factor and $E_{junction}$ in a bulk NAND cell. The scaling limit due to the junction leakage by high $E_{junction}$ is 13nm generation.

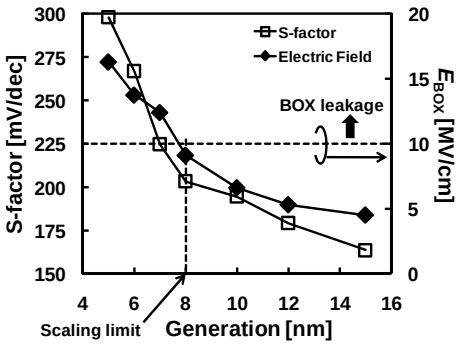

Fig. 9 Scaling trend of the S-factor and E_{BOX} in a SOI NAND cell. Compared with the bulk cell, the scaling limit of the SOI cell extends to 8nm generation.

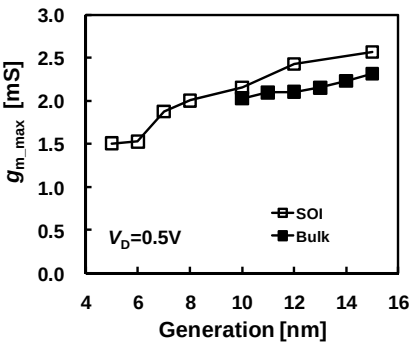

Fig. 10 Scaling trend of the maximum g_m in the bulk and SOI NAND cells.