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Multi-Level Phase-Change Memory Cells with SiN or Ta_2O_5 Barrier Layers

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ABSTRACT

We compare the effects of SiN and Ta_2O_5 barrier layers in multi-level phase-change random access memory (PCRAM) cells. The effects of the SiN and Ta_2O_5 barrier layers on the multi-level switching performance were observed through electrical and thermal analyses.

INTRODUCTION

PCRAM is a robust non-volatile memory (NVM) due to its fast read, write and erase speeds, good scalability and ability to exhibit multi-level behaviour [1]. However, research pertaining to the multi-level capabilities of PCRAM cells is lacking.

In this paper, we report further improvement of the multi-level characteristics of a PCRAM cell, and compare the effects of two different dielectrics (1.5 nm of SiN and 1.5 nm of Ta_2O_5) sandwiched in between a graded $Ge_2Sb_2Te_5$ (GST) stack in a multi-level PCRAM cell. Electrical and thermal analyses were used to explain these effects. Devices with SiN barrier layer fabricated here were compared with devices having a Ta_2O_5 barrier layer [2].

DEVICE FABRICATION

Fig, 1(a) shows the process flow of the device fabrication. 200 nm of TiW (bottom electrode) was first deposited on thermally grown SiO_2 on Si wafer. A 1 □m contact hole was then defined, followed by the deposition of the graded GST stack. The graded GST stack consisted of 25 nm sputtered GST, followed by a 1.5 nm layer of SiN. A further 25 nm of nitrogen-doped GST (NGST) and a 10 nm capping layer of TiW were then deposited to complete the GST stack. The NGST was formed by sputtering GST composite target in N_2/Ar ambient. The nitrogen concentration in NGST was 3.5 atomic percent. SiO_2 dielectric and TiW (top electrode) were then deposited. Fig. 1(b) shows a schematic of the device cross-section, while Fig. 1(c) confirms the presence of the SiN dielectric layer in the graded GST stack.

RESULTS AND DISCUSSION

A. Electrical Characterisation

Fig. 2 is a Resistance-Time plot which shows the three distinct multi-level states (State I, State II and State III) in both the SiN and Ta_2O_5 multi-level devices. The 1st Reset pulse switches the device to State II, the 2nd Reset pulse switches the device to State III, and the Set pulse crystallizes the device to form State I [2].

Fig. 3 shows the *I-V* plots of both the SiN and Ta_2O_5 devices. The three gradients in each *I-V* plot correspond to the three multi-level states of both the respective devices. The difference in the threshold switching voltages (indicated by the dashed lines) of the SiN and Ta_2O_5 devices can be attributed to the difference in resistivities of the respective dielectrics. The electrical resistivity of Ta_2O_5 (~ 10^7 Ωm) [3] is lower than that of SiN (~ 10^9 Ωm) [4]; thus, accounting for the higher threshold switching voltages of the devices with SiN barrier layer.

Fig. 4. illustrates the Reset operation of one of the SiN devices. The resistance window between each consecutive state is roughly 10 times. Fig. 5. shows a comparison between the Set and Reset operations of the Ta_2O_5 and SiN devices. Both types of devices have good resistance windows between consecutive states.

Fig. 6(a) shows the endurance cycling of both the Ta_2O_5 and SiN multi-level devices. It is clear that the SiN device has a better endurance than its Ta_2O_5 counterpart which fails after 400 cycles. Fig 6(b) further shows the endurance of the same SiN device for 10^4 cycles. It is evident that the SiN device has a good potential of displaying high endurance in multi-level PCRAM cells.

B. Thermal Analysis

A two-dimensional finite element analysis was performed to obtain temperature profiles of each phase change material (PCM) layer of both the Ta_2O_5 and SiN devices. Fig. 7 shows the temperature profiles of both the multi-level devices during each pulsing condition.

Fig. 7(a) shows the temperature profiles, during the 1st Reset pulse, of the SiN and Ta_2O_5 devices respectively**.** Thermal isolation is crucial, especially during the 1st Reset pulse, to ensure the coexistence of both amorphous NGST and crystalline GST [2]. Thus, the temperature in the GST layer has to be above 145 ºC, while that of the NGST layer has to be above 620 ºC, to ensure that this intermediate resistance level (State II) exists [2]. The higher temperature profiles of the Ta_2O_5 device suggest that a lower 1st Reset pulse could still switch the device to State II.

The temperature profile plots in Fig. 7(b) are obtained during the 2nd Reset pulse of the respective devices. The higher temperature profiles of the PCM layers in the Ta_2O_5 device is again apparent, and suggests that the device could switch to State III using a lower voltage pulse.

Fig. 7(c) shows the temperature profile plots of the Set pulses applied to the respective devices. The pulsing conditions of both devices for the Set operation are similar.

From these temperature plots we can gather that the Ta_2O_5 devices can be switched to a different state using lower voltage pulses as compared to the SiN devices; this is despite the higher thermal conductivity of SiN (0.075 W/mK) [5] compared to that of Ta_2O_5 (0.026 W/mK) [6]. The lower thermal conductivity of Ta_2O_5 coupled with its lower electrical resistivity, allows the Ta_2O_5 devices to experience better thermal isolation using a lower voltage pulse. This translates to lower power consumption for Ta_2O_5 devices using a 1.5 nm barrier layer thickness.

CONCLUSION

A comparative study was done between SiN and Ta_2O_5 multi-level PCRAM cells using a 1.5 nm barrier layer thickness. Although multi-level devices with SiN barrier layer showed better endurance, the Ta_2O_5 multi-level devices had better thermal isolation at lower voltage pulses, and required less power for multi-level switching than their SiN counterparts. A thinner SiN barrier layer (< 1.5 nm) could be employed in future work, to lower the pulsing voltages of multi-level PCRAM devices with SiN barrier layer; thereby, lowering power consumption of the SiN device.

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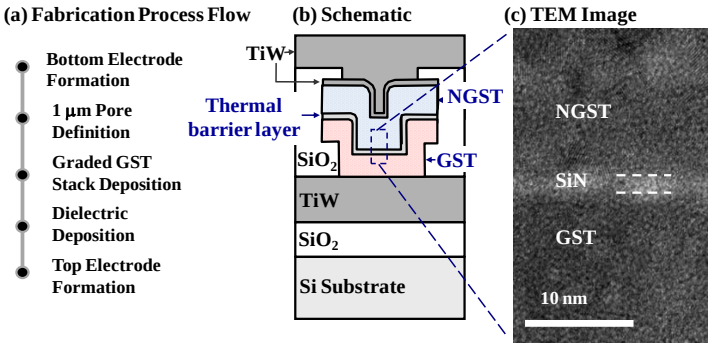

Fig. 1. (a) Process flow used for device fabrication, (b) Schematic of multi-level PCRAM devices, and (c) TEM image of NGST and GST phase change materials sandwiching a SiN barrier layer.

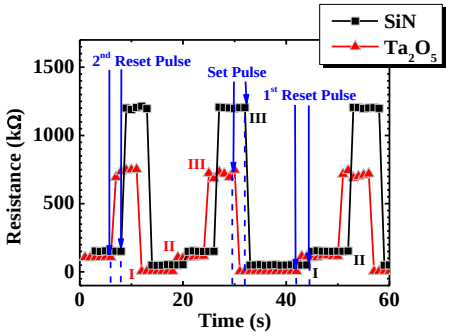

Fig. 2. Resistance-time plot showing three states in multi-level Phase-Change Memory devices with SiN and Ta_2O_5 barrier layers.

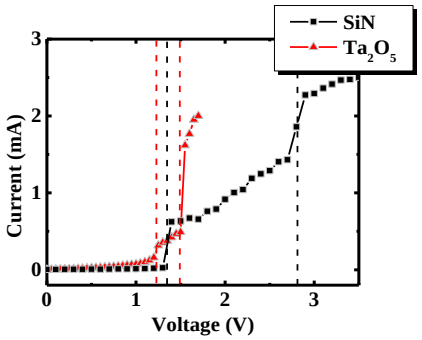

Fig. 3. DC *I-V* sweeps of both SiN and Ta_2O_5 multi-level devices showing threshold switching characteristics.

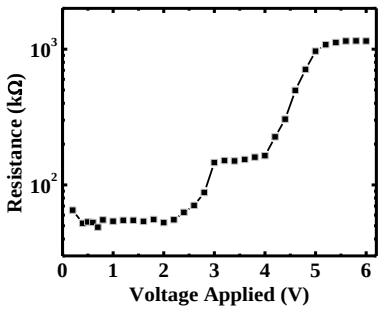

Fig. 4. Reset curve (S curve) of a typical multi-level phase-change memory cell with SiN barrier layer.

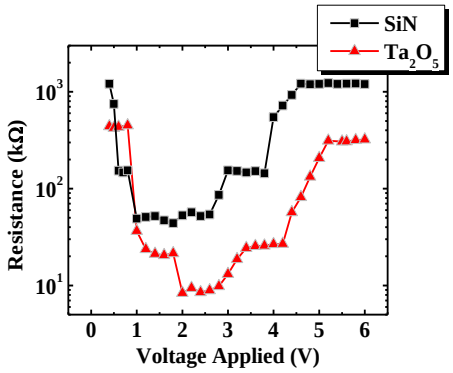

Fig. 5. Set curve (U curve) of both multi-level devices with SiN and Ta2O5 barrier layers.

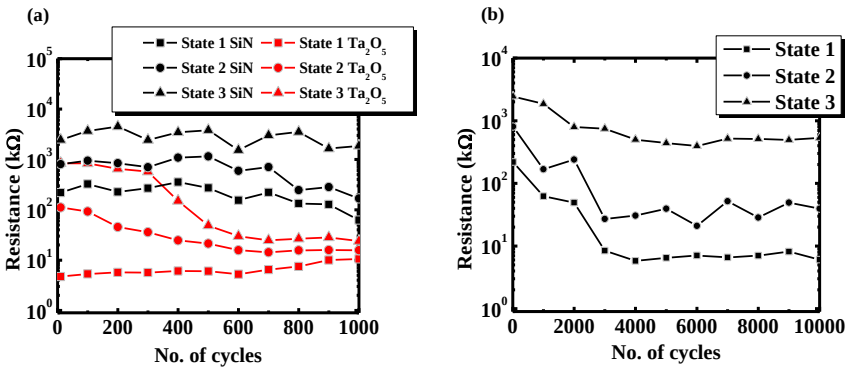

Fig. 6. (a) Endurance cycles of both SiN and Ta2O5 multi-level devices, and (b) the complete Endurance cycle of the same SiN multi-level device.

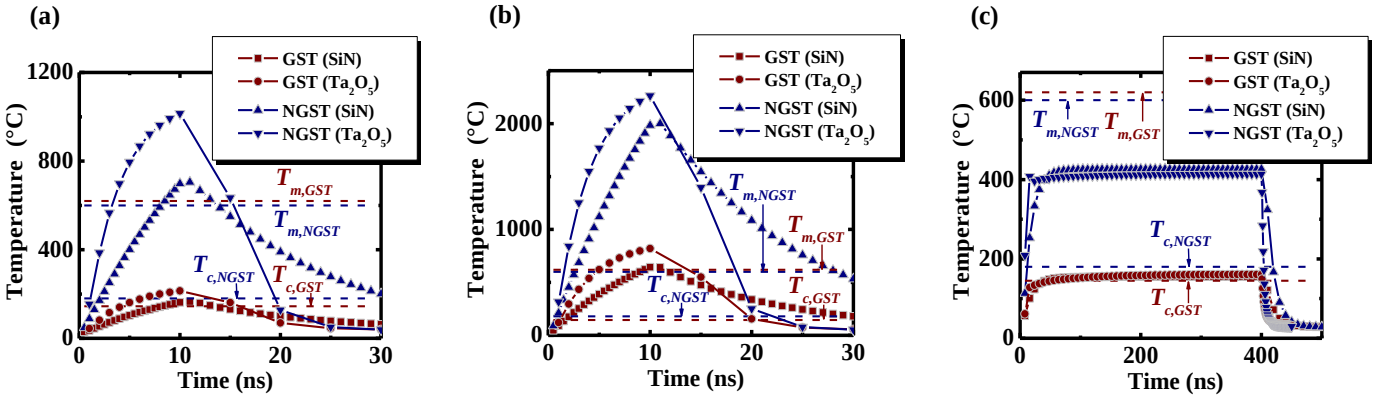

Fig. 7. Plots of Temperature Profile for devices with SiN and Ta_2O_5 barrier layer during the (a) 1st Reset Pulse (4 V 10 ns), (b) 2nd Reset Pulse (6 V 10 ns), and (c) Set Pulse (1.5 V 400 ns).