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Design and Optimization of Program and Restore Operations in CMOS-Compatible Nonvolatile Latch

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1. Introduction

Low-power transceivers for short-range communication systems demand a nonvolatile memory to provide calibration methods of RF/analog circuits against PVT variations, and accelerate the start-up sequence for the battery life extension. The primary requirements for the nonvolatile memory in these applications are 1) self-operated latch with an instant-on operation [1], and 2) manufacturability by CMOS-compatible technology with minimum additional process overheads. In this paper, we present the principle, design and evaluation results of a nonvolatile latch (NV-L) fabricated in standard CMOS technology.

2. Principle and Design of NV-L

The principle of the proposed CMOS-compatible nonvolatile memory utilizes the channel hot-electron trapping at the transistor gate sidewall as shown in Fig. 1 (a). In a standard 1.8V 0.18μm CMOS technology, a large amount of channel hot-electrons are generated when the drain voltage, V_{DS}, over 4.0V is applied while the gate voltage, V_{GS}, is biased to 1.8V as shown in Fig. 1 (b). After the application of V_{DS}=4.4V for 5 minutes, a shift of the threshold voltage, equal to 0.91V, is observed as shown in Fig. 1 (c); on the other hand, no threshold shift is observed for the program disturb condition as is depicted in Fig. 1 (b). In the measurement of threshold voltage after the programming, the source and drain are interchanged since hot-electrons are trapped near the sidewall of drain, and the associated threshold voltage shift becomes larger when the trapped charge is located near the source. Although the programming time of 5 minutes is impractical for many applications, it can be reduced to 10μsec/bit with additional processes [2].

To optimize the drain voltage for the programming, the relationship between the threshold voltage shift and programming voltage is evaluated as shown in Fig. 1 (d). The threshold voltage shift increases according to the increase of the programming voltage. However, when the programming voltage becomes over 4.8V, the device is susceptible to breakdown. As a result, programming voltage is determined as 4.4V.

The memory cell in NV-L and operations for program and restore are illustrated in Fig. 2. The memory cell has a differential 2-transistor structure, where the one of the cell transistors is programmed, and the other cell transistor is un-programmed according to the data. The source side of

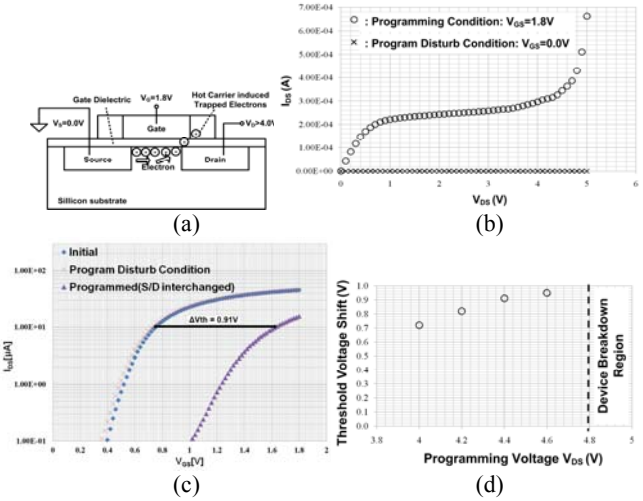

Fig. 1: Memory cell operation (a) Nonvolatile memory cell structure, (b) I-V characteristics in programming condition, (c) I-V characteristics comparing initial and programmed cell, (d) Relationship between programming voltage and threshold voltage shift

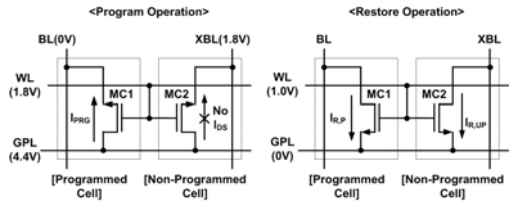

Fig. 2: Program and restore operations of memory cell

Table I Applied voltages in program and restore operations

Operation	Condition in WL		V_{WL} (V)	$V_{BL/XBL}$ (V)	V_{GPL} (V)
Program	Selected WL	Programmed Cell	1.8	0.0	4.4
		Non-programmed Cell	1.8	1.8	4.4
	Unselected WL		0.0	0 or 1.8	4.4
Restore	Selected WL		1.0	Precharged	0.0
	Unselected WL		0.0	Precharged	0.0

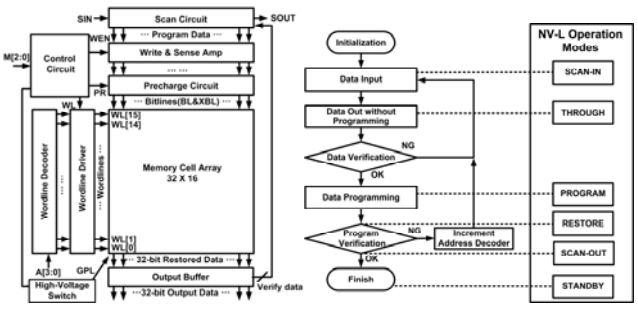

Fig. 3: (a) Memory cell and architecture of 32-bit NV-L, (b) Typical operation sequence of NV-L.

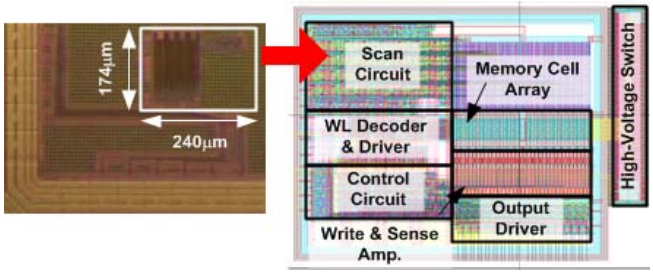

Fig. 4: NV-L Prototype die photo and layout.

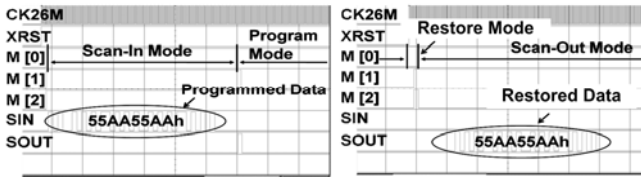

Fig. 5: Measurement result of program and restore operation.

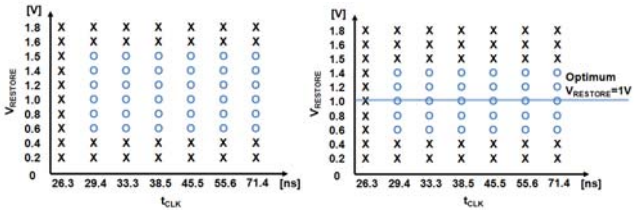

Fig. 6: (a) Shmoo plot of restore voltage versus operation speed taken 1 minute after programming at 25°C, (b) Shmoo plot of restore voltage versus operation period taken after temperature stress of 150°C for 24 hours.

the memory cell is not grounded but is connected to a global plate line (GPL) to apply the high programming voltage through this line. In the program operation, it should be noted that since the wordline (WL) voltage (V_{WL}) is 1.8V, the bitline (BL) voltage (V_{BL}) of 1.8V is applied to the un-programmed cell. In the restore operation, wordline voltage is set to the 1.0V, which corresponds to the averaged threshold voltage for the programmed and non-programmed (disturbed) cells, and the bitline voltage difference is sensed through the precharging of BL and XBL to V_{DD} (1.8V) and subsequent discharging from the un-programmed cell.

The bias voltages of the selected and unselected cells are summarized in Table I. From Fig. 1 (b) and (c), it is proved that the influence of program disturbance for the unselected-WL and selected-GPL cell is negligibly small. The influence of disturbance during the restore operation is negligible since the drain voltage of 1.8V does not generate significant channel hot-elections. When the restore voltage ($V_{restore}$) is applied to the wordline (WL), the voltage difference between V_{BL} and its complement V_{XBL} is generated. Then the voltage difference is amplified to the full rail to rail by an internal differential sense amplifier.

The primary issue in this channel hot-electron trapping scheme is that de-trapping electrons is not valuable; therefore, this memory cell has only one-time programmability. To provide sufficient programmability, the architecture of 32-bit self-operated NV-L to realize multiple-time programmability up to 16 cycles is shown in Fig. 3 (a) and its typical operation is illustrated in Fig. 3 (b). The memory cell is operated to receive input data in Scan-In mode, verify the received input data in Through mode, program the received data in Program mode, read the stored data in Restore mode and output the stored data in Scan-Out mode respectively. According to each operation in the entire sequence, one of 6 operation modes is selected by 3-bit mode selection code M[2:0]. In these sequences, Program and Restore operation should be optimized to maximize the device reliability.

3. Experimental Result

A prototype NV-L is designed in a standard 1.8V 0.18μm CMOS technology without any additional processes. The gate length and width of the memory cell transistor are 0.18μm and 0.42μm, respectively. The active area of entire 16-program cycle 32-bit NV-L has 240μm x 174μm as shown in Fig. 4. The measurement waveforms of the NV-L operations are shown in Fig. 5, where the programming sequence is shown in the left side. The programming mode continues 5 minutes with programming voltage of 4.4V, and the Restore operation is verified after a temperature stress of 150°C for 24 hours. The verified data has been observed through the Restore and Scan-out mode operations as shown in the right side. The proper operation of the NV-L has been observed after the stress.

To verify the restore voltage $V_{restore}$, Shmoo plots have been taken for the case after 1 minute power down from programming at 25°C in Fig. 6 (a), and for the other case after the temperature stress of 150°C for 24 hours in Fig. 6 (b). The wireless application demand the operation speed up to 38nsec (26MHz), and both plots present the sufficient speed margin in Restore operation. The optimum value of restore voltage as shown in Fig. 6 (b) is 1.0V, which corresponds to the average value of threshold voltage for the programmed and un-programmed cells.

In conclusion, we have successfully designed and evaluated a prototype 16-program cycle 32-bit NV-L in a standard 0.18μm 1.8V CMOS technology applicable to RF/analog calibrations.

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References

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[2] PermSRAM®, NSCore Inc. Product Description, *Online: http://www.nscore.com/product/permsram. html.*