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SET polarity dependent resistive switching memory characteristics using $IrO_x/GdO_x/WO_x/W$ structure

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1. Introduction

With conventional nonvolatile floating gate memory approaching certain technical and physical limits in the future, alternative nanoscale nonvolatile memory is becoming interesting subject. Recently, resistive switching random access memory (ReRAM) is showing alternative choice for the potential in future replacement of DRAM and conventional floating gate memory. Many materials have been demonstrated to possess ReRAM characteristics such as $GeSe_x$, NiO, WO_x, ZnO, ZrO_x, HfO_x, TaO_x, TiO_x, and so on [1-6]. However, the rare-earth oxide such as Gd_2O_3 for ReRAM device is reported infrequently [7]. The reason to choose Gd_2O_3 is transparency material in nature, which can be used in future nanoscale nonvolatile memory for flexible display panel. Although many ReRAM devices have been studied but formation polarity as well as SET polarity dependent improved resistive switching memory performance in an $IrO_x/GdO_x/WO_x/W$ structure has not yet been reported. This novel ReRAM device shows excellent repeatable switching and 10 years data retention at 85°C under a small positive SET polarity of 1.8V.

2. Experiment

Tungsten (W) metal as a bottom electrode (BE) was deposited by sputtering on SiO_2/Si 8 inch substrate. To form the ReRAM device, the SiO_2 layer with a thickness of ~150 nm was deposited. Then a small via with an active area of 2x2 μm^2 was fabricated using standard lithography. Photo-resist was used to deposit resistive switching material and top electrode (TE). Then high-κGd_2O_3 with a thickness of 15 nm was deposited by E-beam evaporation using pure Gd_2O_3 grains with sizes of 2-3 mm. Then IrO_x as a TE with a thickness of ~300 nm was deposited by rf sputtering. The lift-off process was used to fabricate the ReRAM device. Schematic view of our $IrO_x/GdO_x/WO_x/W$ ReRAM device is shown in Fig. 1. Fig. 2 shows cross-sectional high-resolution transmission electron microscope (HRTEM) image of our novel $IrO_x/GdO_x/WO_x/W$ ReRAM device with a via size of 2x2 μm^2. Due to a small size, the device was prepared by FIB for TEM observation. The thicknesses of the GdO_x and WO_x layers were ~ 15 and 5.5 nm, respectively. The EDX spectra confirm the presence of expected elements of Ir, Gd, W, and O in respective layers (Fig. 3). The W-O bonding with an energy peak at 35.48 eV was confirmed by X-ray photoelectron spectroscopy [Fig. 4(a)]. The WO_3 layer was formed at the W/GdO_x interface during deposition of GdO_x and IrO_x layers. It is also advantage to control resistive switching phenomena using GdO_x/WO_x bilayer structure. Fig. 4(b) represents the chemical bonding states of Gd_2O_3 film. The Gd 3d5/2 and Gd_2O_3 3d5/2 peaks are at 1186.73 eV and 1189 eV, respectively, which proves Gd: Gd_2O_3 mixture. Fig. 5 shows the SET polarity dependent formation process of the pristine devices. The leakage currents are 1.47×10^{-7} and 1.94×10^{-10} A at the read voltages (V_{read}) of +2V and -2V, respectively. The asymmetric leakage currents are due to different work functions of W (Φ_m~4.6 eV) and IrO_x (Φ_m~5.2 eV). To activate the resistive switching behavior, the formation voltages of approximately +3.4V and -6.4V are needed under positive and negative polarity, respectively, with a current compliance (I_{CC}) of 100 μA. After 1st RESET process, the resistive switching characteristics are observed.

3. Results and discussion

Fig. 6 shows the typical bipolar switching current-voltage (I-V) characteristics after negative formation process. The sweeping voltages with an I_{CC} of 1 mA are as follows: 1→4. The SET (V_{SET}) and RESET (V_{RESET}) voltages are -2.4 and +1.9V, respectively. The current transports of high resistance state (HRS) and low resistance state (LRS) show Schottky emission and Ohmic behaviors. Under negative polarity on TE ($-V<V_{SET}$), the oxygen ions (O^{2-}) will migrate from GdO_x layer toward WO_x layer. On the other hand, the oxygen vacancies (V_o) will migrate from WO_x layer toward GdO_x layer and the oxygen vacancy filament will form in the GdO_x layer and sets a LRS. The conducting filament will be ruptured by applying positive voltage ($+V>V_{RESET}$) on the TE. It is expected that the filament is ruptured by joule heating process. That's why the DC cycles uner negative SET polarity are not so stable. On the other hand, excellent 700 consecutive DC cycles are observed after positive formation process (Fig. 7). The V_{SET} and V_{RESET} are +1.8V and -1.8V, respectively. Both HRS and LRS show trap-charge controlled current transport mechanisms. It suggests that the current transport is controlled by initial barrier height, which depends on Φ_m of the electrodes. Improved repeatable I-V characteristics are due to barrier height control current transport mechanism. Fig. 8 shows tight distribution of (a) HRS/LRS and (b) SET/RESET voltages with cycle-to-cycle (C-C) and device-to-device (D-D). Average LRS and HRS are 8.6 kΩ and 206.2 kΩ, respectively. Tight distribution of the V_{SET} from +1.7V to +1.9V and V_{RESET} from -1.6V to -1.9V is observed. Fig. 9 shows good program/erase endurance of $>10^4$ cycles. A good resistance ratio of >10 is obtained. Fig.10 shows excellent read endurance characteristics of 10^5 times at a read voltage of +0.1V. Fig.11 shows the retention characteristics of the memory device at room temperature (RT) and 85°C under negative SET polarity. The device shows good retention with maintaining a high resistance ratio of $>10^3$. Excellent data retention characteristics are also observed for positive SET polarity at RT and 85°C (Fig.12). Extrapolation of data retention with an acceptable resistance ratio of ~10 can guarantee 10 years nanoscale nonvolatile memory applications in future. Due to improve resistive switching characteristics of $IrO_x/GdO_x/WO_x/W$ structure under positive SET polarity, this structure could be used in future nanoscale nonvolatile memory for flexible display panel.

4. Conclusions

Novel memory device in an $IrO_x/GdO_x/WO_x/W$ structure under negative/positive SET polarity is investigated. Improved resistive switching characteristics with repeatable cycles, SET/RESET voltages, HRS/LRS, and endurance are obtained under positive SET polarity. Excellent read endurance (10^5 times) and extraplotted 10 years data retention at 85°C under positive SET polarity are useful in future nanoscale transparency nonvolatile memory applications.

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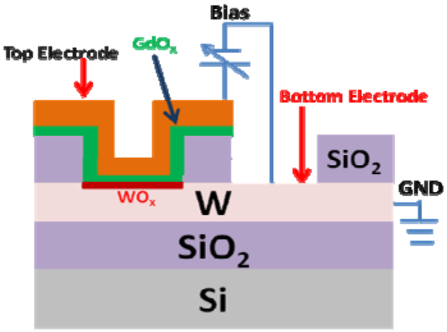


Fig. 1 Schematic view of the resistive memory device using $IrO_x/GdO_x/WO_x/W$ structure. The device size is 2x2 μm^2. During deposition of GdO_x and IrO_x, the interfacial WO_x layer was formed.

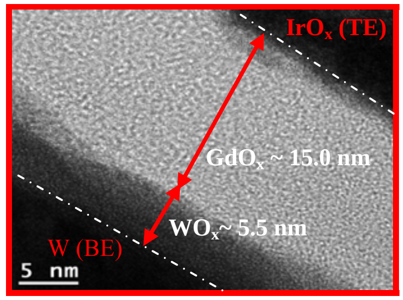


Fig. 2 Cross-sectional HRTEM image of $IrO_x/GdO_x/WO_x/W$ memory device. Thickness of GdO_x layer ~ 15 nm and WO_x layer ~ 5.5 nm. So GdO_x/WO_x bilayer is observed.

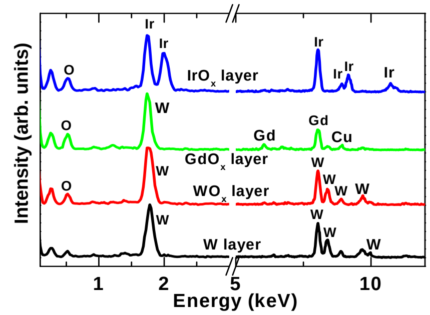
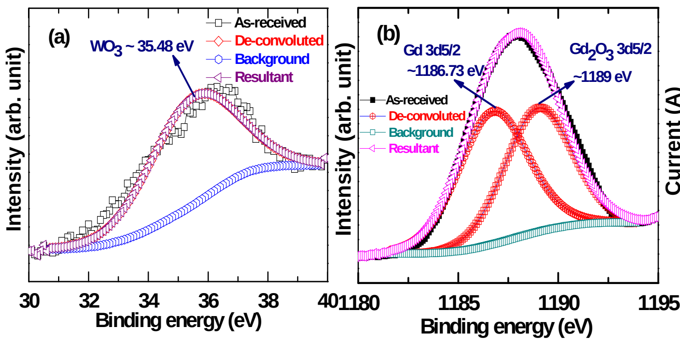
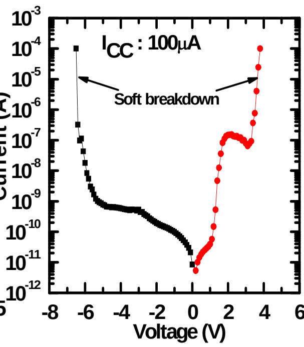


Fig. 3 Energy dispersive X-ray spectra (EDX) show Ir, Gd, W, and O elements from Fig. 2. It proves layer-by-layer structure with presence of GdO_x resistive memory layer.





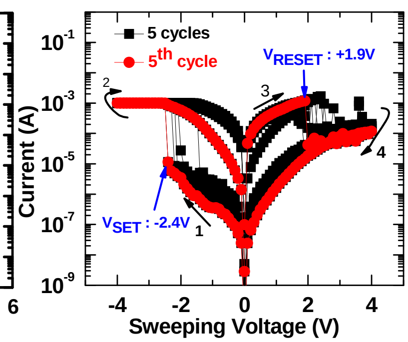


Fig. 4 XPS characteristics of (a) WO_3 and (b) GD*3d* in W and GdO_x layers, respectively for our $IrO_x/GdO_x/WO_x/W$ structure. It is interesting to note that Gd is mixed with Gd_2O_3 film. It suggests that oxygen vacancies are possible easily.

Fig. 5 Typical formation of both positive and negative voltages on TE of $IrO_x/GdO_x/WO_x/W$ memory device.

Fig. 6 Typical I-V hysteresis loop of $IrO_x/GdO_x/WO_x/W$ memory device of negative SET polarity with current compliance of 1mA.

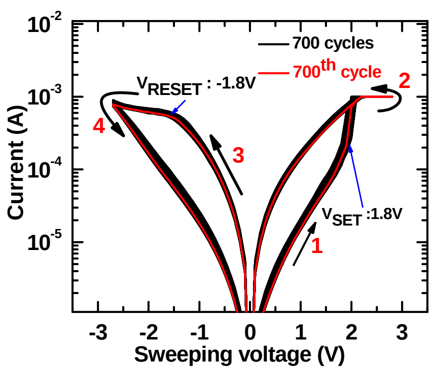


Fig. 7 Excellent repeatable I-V hysteresis loop of $IrO_x/GdO_x/WO_x/W$ memory device up to 700 cycles under negative SET polarity. The resistance ratio is >10, which is very useful for application.

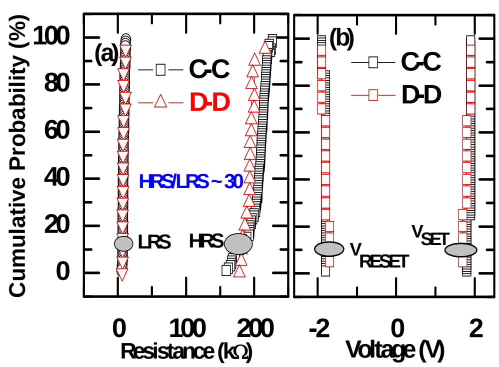


Fig. 8 Excellent cumulative probability of (a) HRS/LRS and HRS and (b) SET/RESET voltages with cycle-to-cycle (C-C) and device-to-device (D-D). The device could be operated within ±4V. The formation process was positive polarity.

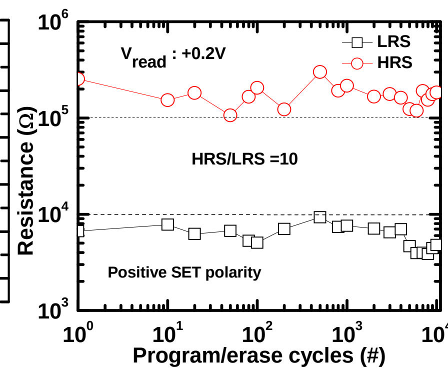


Fig. 9 Program/erase cycles of the $IrO_x/GdO_x/WO_x/W$ memory device with a long endurance of 10^4 cycles at a read voltage of +0.2V.

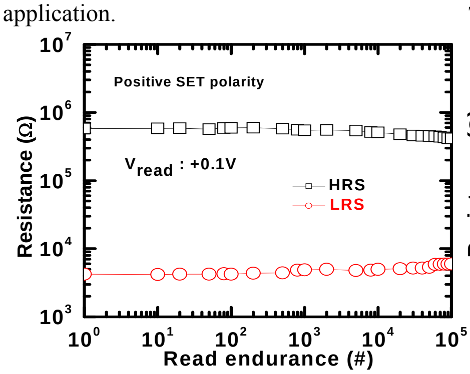


Fig.10 Excellent read endurance of 10^5 times with positive SET polarity at a read voltage +0.1V is observed.

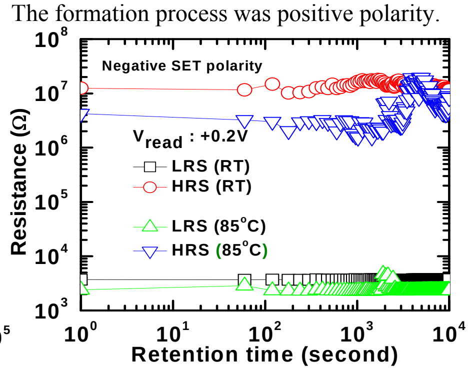


Fig.11 Good retention characteristics with negative SET polarity at 85°C is observed. The resistance ratio is ~10^3 at a read voltage -0.2V is observed.

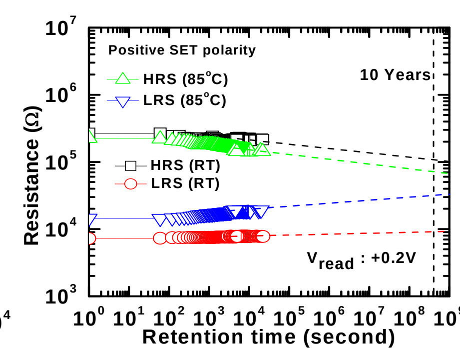


Fig. 12 Excellent retention characteristics with positive SET polarity at 85°C is observed. Extrapolation of data retention can guarantee 10 years nonvolatile memory application.