Improved electrical properties of charge trap flash memories having a patterned surface in a Si₃N₄ trap layer

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1. Introduction

The floating gate (FG) flash memory density has been increased dramatically over the last two decades due to the rapid digitalization of analog information. As a main mobile storage device, NAND flash memory has been advanced to increase the memory density. However, it is expected that the FG device scaling is facing its physical limits due to the scaling limit of gate length and tunneling oxide thickness. In recent years, charge trap flash (CTF) or polysilicon/oxide/nitride/oxide/silicon (SONOS) memory devices are being developed for commercial applications to replace the traditional FG devices in NAND applications around the 30 nm or 2x nm technology node [1, 2]. This is due to the merit of charge storage in discrete traps within Si₃N₄ layer, which prevents charge leakage through a tunnel oxide. However, as the dimension of ONO layer is reduced, it is difficult for CTF device to obtain the abundantly operating memory window because of their insufficient densities of trap states.

In this work, we investigate the enhancement of memory window in CTF memory using by nanosphere lithography (NSL), in which surface of Si_3N_4 trapping layers have been patterned on a nano-size scale using reactive ion etching (RIE). The polystyrene (PS) bead of 500 nm-diameter were used as mask to make patterns in the etching process with CF₄ as the gas source.

2. Experiments

Figure 1 shows the schematic diagram of fabricated metal-aluminum oxide-nitride-oxide-silicon (MANOS) samples with (a) flat surface and with (b) patterned surface at the interface between the Si₃N₄ and blocking layer. All of the processes used for making two capacitors were identical, except for that of surface roughness process at interface between the trapping layer and the blocking oxide layer. Firstly, a 5 nm-thick tunnel oxide layer was deposited on top of silicon at 750 °C by using the low-pressure chemical vapor deposition (LPCVD). And then a 10 nm-thick nitride layer of was deposited using LPCVD at 750 °C, by the reaction of dichlorosilane $(SiCl_2H_2)$ and ammonia (NH_3) gases. Next, a 10 nm-thick blocking layer of Al₂O₃ was deposited for the oxide-nitride-aluminum oxide (ONA) stack using radio frequency (RF) sputter. After depositing the ONA layer, the gate electrode of aluminum (Al) with a 300 µm diameter was deposited on top of the blocking

oxide layer using an electron beam evaporator.

On the other hand, the process for patterned surface sample, as shown in Fig 1(b), is as follows. The wafer deposited ON layers on the p-Si substrate was sonicated in a 175 ml RCA solution (H₂O₂/NH₄OH/DI water=1:1:5) at 75~85°C for 1 hour in order to obtain a hydrophilic surface. Then, the PS bead solution, prepared using a 10 wt% concentration, was diluted in a solution of surfactant Triton X-100/methanol (1:400 by volume) in a ratio of 4:1 to 5:1 by volume before the spin-coating process. The 500 nm PS beads (Duke Scientific Co.) produce a hexagonal close-packed (HCP) monolayer on the Si₃N₄ layer through spin-coating. In order to control the diameter, the PS beads are then etched using RIE with 100 sccm of oxygen at a pressure of 500 mTorr and a RF power of 300 W with an etching time of 420 sec. After that, in order to create the surface roughness, the Si₃N₄ layer are etched using RIE with CF₄ gas at a pressure of 30 mTorr and a RF power of 50 W with an etching time of 3 sec. The thicknesses of the ONA stacks were confirmed to be 5/10/10 nm by spectroscopic ellipsometry.

3. Results and discussion

In order to demonstrate the effect of memory traps density and to compare the performance in MANOS capacitors with the flat surface and the patterned surface at the interface between the Si₃N₄ and blocking layer, the program characteristics are shown in Fig. 2. The flat-band voltage (V_{FB}) shifts are plotted against the program time at different gate voltages from 11 V to 13 V, after the cells were erased at a zero V_{FB} . The maximum V_{FB} shift of the capacitor with patterned surface was observed to be greater than that the capacitor with flat surface at program voltage of 13 V. This result explains that the patterned nitride layer creates a large memory traps at the interface between the nitride and top oxide, so that the higher V_{FB} shifts are occurred. Besides, a V_{FB} shift of 2.5 V, which is large enough for program operation, was observed at a gate bias 12 V with program time of 50 ms for the patterned structure, while the same shift was observed at a gate bias 12 V with program time of 500 ms for the flat structure. It is interesting to find that the operating voltages and times for programming in the patterned structure are always lower than those in the flat structure one.

Figure 3 shows the retention characteristics measured in the programmed and erased states at room temperature for both the flat and patterned samples. The V_{FB} shifts are plotted as a function of the retention time after the cells were either programmed or erased at the same V_{FB} . The program voltage and time are 12 V and 1 s, and the erase voltage and time are -14 V and 1 s for the flat samples, while those of the patterned samples are 12 V and 100 ms. and -14 V and 1 s, respectively. The flat band voltages in both the programmed and erased states were measured up to a retention time of 10^6 s and then extrapolated thereafter to estimate the long-term retention properties for each sample. As a result, the charge decay rates of the flat and patterned samples were calculated to be 40 and 48 V/decade in the programmed state and 32 and 73 mV/decade in the erased state, respectively. Beyond the retention time of 10^9 s (or about 10 years), it is expected that the patterned samples would still show large memory windows.

Finally, we measured the endurance features with an operation window of 2.5 V by observing the V_{FB} shifts with respect to the P/E cycles for the flat and patterned samples, as shown in Fig. 4. For the endurance test, the program voltage and time are 12 V and 500 ms, and the erase voltage and time are -14 V and 1 s for the flat samples, while those of the patterned samples are 12 V and 50 ms, and -14 V and 1 s, respectively. The memory windows of two samples gradually decrease with increasing P/E cycling. The memory window is measured to be about 1 V after $10^4 P/E$ cycles, which indicates that the patterned structure is still in good shape in terms of its endurance. However, endurance properties are not excellent, compared to the reported SO-NOS or MANOS devices with tunnel oxide layer grown by thermal oxidation process. This might be due to the usage of tunnel oxide deposited by LPCVD for our devices. The present experiment was conducted to confirm the feasibility of the proposed structure without optimizations. Optimizing the layers of the MANOS structure should produce further improvements in device performance.

4. Conclusion

In order to enhance the memory window for achieving high-density CTF devices, a novel CTF memory structure having the traps layer patterned surface on Si_3N_4 trap layer is proposed and studied in this work. As a result, the CTF devices by adopting a roughened surface on Si_3N_4 trap layer show the increase of memory window and improved program properties, compared to those with flat surface on the Si_3N_4 layer. In addition, accepted reliability characteristics, such as a data retention of 10 years and an endurance of $10^4 P/E$ cycles, are obtained. This study can provide an alternative process for formation of the trapping layer in future 30-nm or 2x-nm C TF memory devices.

References

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Figure 1 The schematic daigram of SONOS devices (a) with flat surface and (b) with patterned surface.



Figure 2 Program characteristics of the MANOS capacitors with flat surface and patterned surface.



Figure 3 Retention characteristics measured in the programmed and erased states at room temperature for the flat and patterned samples.



Figure 4 Endurance characteristics evaluated to observe the V_{FB} shift as a function of program/erase for the flat and patterned samples.