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Poly Si-TFT Flash Memory with High-k Trapping and Blocking Layer on Glass Substrate for System on Panel

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1. Introduction

Poly-Si thin film transistors (TFTs) have been widely used in active matrix liquid-crystal-displays (AMLCD) and active matrix organic light emitting diode displays (AMOLED) as pixel switching elements because of the higher mobility and improved reliability of these transistors compared to TFTs based on amorphous silicon films [1,2]. SONOS memory device with poly-Si TFT suffers from low programming/erasing (P/E) speed and high operation voltage.

In this paper, we conducted a study of the tunnel barrier engineered (TBE) poly-TFT memory device using high-k HfO_2 and Al_2O_3 as trapping layers and blocking layers, respectively, on glass substrate to improve memory performances, such as program and erase (P/E) speed, data retention, and endurance characteristic.

2. Experiment

The TBE-TFT memory device was fabricated using undoped poly-Si layers on the glass substrate. The crystallization of amorphous Si layer was carried out by the excimer laser annealing system. The large silicon grain was obtained by the ELA crystallization method. Also, the ELA method showed the clearest and narrowest grain boundaries as shown in Fig. 1(a). As a tunneling barrier of Metal/Al_2O_3/HfO_2/SiO_2/Si_3N_4/SiO_2/Si (MAHONOS) structured memory device in the Fig. 1(b), the 7-nm- thick SiO_2, 7-nm-thick Si_3N_4 and 7-nm-thick SiO_2 layers were successively deposited on the recessed Si channel at room temperature by the RF sputtering method. Then, the HfO_2 film as a charge trap layer of 8 nm thickness and the Al_2O_3 film as blocking oxide layer of 15 nm thickness on the ONO tunnel barrier were deposited using the RF sputter system at room temperature. Finally, the Ni gate electrode with a thickness of 150 nm was deposited by e-beam evaporation. The electrical characteristics of the TBE-TFT memory device were measured using the HP-4156B semiconductor parameter analyzer system and the HP-8110A pulse generator.

3. Results and Discussion

Fig. 2 shows the transfer characteristics of the TBE-TFT memory device on glass substrate after program and erase (P/E) operations conducted by an applying gate bias of +20 and -20 V for 1s, respectively. According to the results above, we were able to determine that the TBE-TFT memory on glass substrate has good electrical characteristics, such as high on/off current ratio (1×10^8), low subthreshold swing (254 mV/dec) and good memory operation.

Fig. 3 shows the P/E characteristics of TBE-TFT memory device under the gate voltages of ±18 V, ±19 and ±20 V. Based on the results above, we were able to find out that TBE-TFT memory devices revealed a large memory window of 6.5 V at +20 V/1s and 3.29 V at -20 V/1 s for programming and erasing operations, respectively. These improvements of high P/E speed and large memory window of our study were attributed to the enhanced tunneling sensitivity of engineered tunnel barrier (ONO). Additionally, the HfO_2 and Al_2O_3 for charge trap and blocking oxide layers with high dielectric constant and large conduction band off-set enhance the tunneling current and device performance. Therefore, this structure results in the increase of tunneling current from the Si substrate to the charge storage layer due to a larger band bending through a voltage drop across the tunnel barrier.

Fig. 4 shows the data retention characteristics of the TBE-TFT memory device. The initial memory window was 2.63 V under +19 V at 100 ms and -20 V at 1 s operation. Meanwhile, the memory window after 10 years was slightly reduced to 2.03 V. From these results, the charge loss rate after 10 years was estimated to be about 22.8 %. This improvement is mainly attributed to the suppressed leakage current as the physical oxide thickness (POT) increases in case of the engineered tunnel barriers.

Fig. 5 shows the endurance characteristics of TBE-TFT memory device. The memory window is reduced from 3.44 V to 2.05 V after P/E operations of 10^3 cycles. The upward threshold voltage shift may be caused by the creation of interface traps and the trapping of charges in the tunneling oxide.

4. Conclusion

In this paper, we developed the TBE-TFT memory device on glass substrate with high-k HfO_2 trapping layer and Al_2O_3 blocking layer for SOP application. The TBE-TFT memory device based on glass substrate demonstrated a fast P/E speed, large memory window, good retention time and endurance. As a result, we can conclude that engineered tunnel barrier flash memory devices are considered to be

promising candidates for highly integrated SOP (System on Panel) applications.

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References

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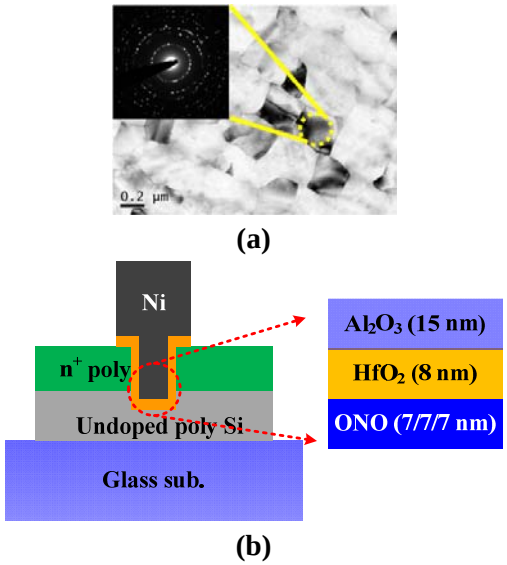

Fig. 1. (a) TEM image of microcrystal-line silicon films formed on glass using ELA method and electron beam diffraction patterns within the grain. (b) Recess-channel TBE-FET memory device on glass substrate and tunnel, trap and blocking layers, respectively.

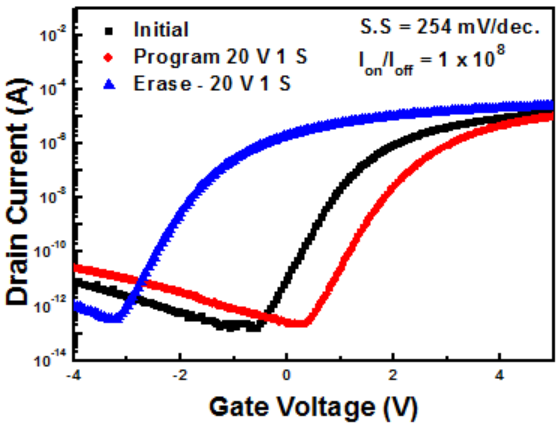

Fig. 2. Transfer and P/E characteristics of a TBE-TFT memory device on glass substrate. The device was programmed and erased by applying +20 and -20 V, respectively.

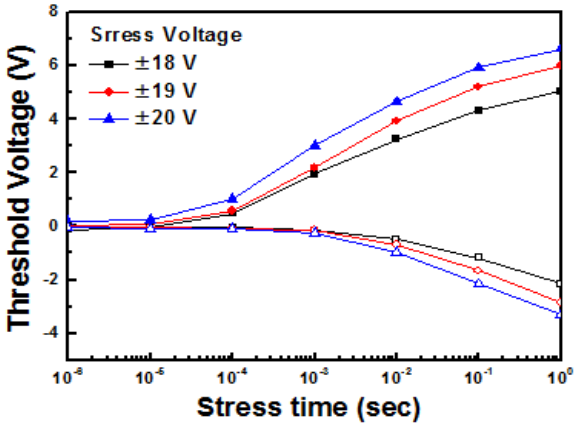

Fig. 3. Programming and erasing characteristics of a TBE-TFT memory device on glass substrate.

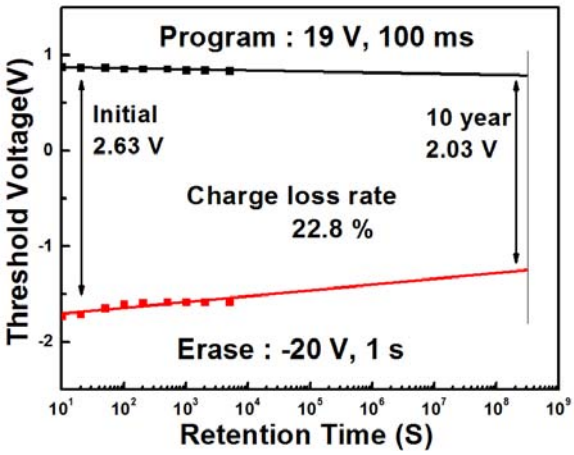

Fig. 4. Charge retention characteristics of TBE-TFT memory device on glass substrate. The device was programmed and erased by applying +19 V at 100 ms and -20 V at 1 s, respectively.

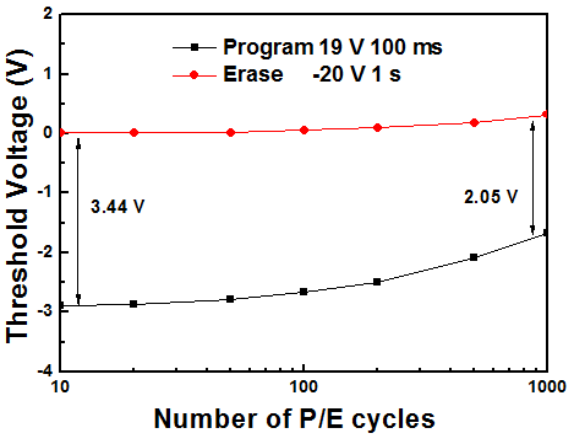

Fig. 5. Endurance characteristics of TBE-TFT memory device on glass substrate. The device was programmed and erased by applying +19 V at 100 ms and -20 V at 1 s, respectively.