Electrical Property of DNA FET –Charge Retention Property–

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1. Introduction

Moore's Law that the integration will be four times every three years has reached the stage not approved any longer for the research and development of ULSI (ultra-large scale IC). Although complementary metal oxide semiconductor (CMOS) circuit has been made via top-down technology, the fabrication process becomes difficult toward the coming generation whose gate length is smaller than 20nm. The new materials such as carbon nanotube [1] and graphene [2] are expected to substitute for Si [3]. Deoxyribonucleic acid (DNA) has a characteristic to flow electric current, and in addition, forms nano-structure with a self-organization [4]. DNA also becomes one of the potential candidates for the material beyond CMOS. In addition, DNA is known to have the semiconductor characteristic, and it shows the transistor characteristic [5]. We examined the conduction characteristic of DNA field effect transistor (FET) with the Si gate [6]. However, further examination related with electrical characteristics is needed to accommodate the conditions beyond CMOS. In the present study, we investigated the charge retention property of the FET in Si(Gate)/SiO₂/DNA structure.

2. Experimental method

Fig.1 shows schematic configuration of the DNA transistor. A 4µm-thick and n- type SOI with resistivity of 40~60 Ω cm was served to fabricate DNA FET. The source/drain with a thickness of 150nm was formed by etching the SOI film. We attached an epoxy function through hydrosilylation of allyl glycidyl ether (AGE) on the Si surface of the source and drain electrodes. We connected both Si electrodes with long-SH-DNA of 400bp. The length of the DNA is 136nm. Long-SH-DNA was prepared by a PCR technique using 5'-disulfide-modified DNA primers and λ -DNA as a template.



Fig. 1 Schematic configuration of DNA transistor.

3. Results and discussion

Fig.2 shows the dependence of the drain current I_d on the time kept in the atmosphere. Only for the sample with a channel length of L=120nm that is shorter than the DNA length, the current has increased with the time. For the channel length of 120nm, DNA was bridged between the Si electrodes and the drain current increased with the time because of decrease of water molecules in DNA. For the channel length longer than 120nm, the DNA was not bridged between the electrodes, and the drain current did not flow. Fig.3 shows the dependence of drain current on the drain voltage at the gate voltage of 0 to -5V. It is found that the DNA FET with Si source/drain electrodes shows the hole conduction and the drain current was successfully controlled by the gate voltage application. In the beginning of the Id-Vd characteristics, however, the currents related with the space change limited currents (SCLC) were observed. The origin of the SCLC is thought to be the charge trap in the DNA. These characteristics have a close relation with the arrangement of the DNA. The hole



Fig. 3 Dependence of drain current I_d on the drain voltage at the gate voltage of 0 to -5V. (W = 100 µm, L = 120 nm)



field-effect mobility was calculated to be 2.46×10⁻³ cm²/Vs assuming that the channel was entirely covered with DNA. However, it will be improved to be a few cm^2/Vs [7] assuming the DNA Nano-wire FET. Next, we examined the current stability and charge retentivity. Fig.4 shows the dependence of the drain current I_d on the time of voltage application. Although the drain current fluctuates in several hours in the beginning of the voltage application, it approaches a constant value with time. Fig.5 shows the dependence of the drain current on the repetition number of the measurement for the DNA FET and the conv. poly-Si TFT. The drain current of the DNA FET increases for every measurement, although it is constant for the conv. poly-Si TFT. This phenomenon indicates that the charge trap in the DNA occurs. We tried to insert the refresh process before every measurement. The detrap of the charge was performed by applying -50V to the gate electrode under non-voltage- application to the source and drain electrodes. Fig.6 shows the dependence of the drain current on the repetition number of the measurement for the DNA FETs without and with refresh process. The current increase after every measurement was not observed for the DNA FET with refresh process. It is thought that there are many trap sites in the DNA. Fig.7 shows the detrap mechanism of electrons in the DNA. There are electron trap sites in the band-gap of the DNA. The hole emission, which is minority carrier of the drain n-Si, occurs via direct-tunneling of AGE film and the hole current flows in the DNA. The origin of the hole-current is the mutual exchange of the sites for electrons and holes. Therefore, the electrons in the DNA channel were trapped in the DNA band-gap. By application of the negative voltage to the gate, the electrons, which energy is larger than E_{f} , are detraped and the original I_d-V_d characteristic is recovered.



3. Conclusions

The DNA FET with Si gate and Si source/drain structure was successfully fabricated. The drain currents were controlled by the gate application. However, SCLC characteristics related with the charge trap in the DNA was observed. The increase of the drain currents was also observed in the repeated measurement under the same bias condition to the gate and source/drain. By inserting the refresh process before every measurement, the increase of the drain currents was not observed. The origin of this phenomenon is the charge trap and detrap in the DNA, and also the charge retention property in the DNA was observed for the first time in the world.

References

- R. Martel, H.-S. Philip Wong, K. Chan and P. Avouris, IEEE International Electron Device Meeting (IEDM) Tech. Dig., 2001,159-162.
- [2] K. Nagashio, T. Nishimura, K. Kita and A. Toriumi, IEEE International Electron Device Meeting (IEDM) Tech. Dig., 2009, 565-568.
- [3] International Technoligy Roadmap for Semiconductors (ITRS) 2009 Edition.
- [4] B. Xu, P. Zhang, X. Li, and N. Tao, Nano Lett. 4, 1108 (2004).
- [5] M. D. Ventra, M. Zwolak, Encyclopedia of Nanoscience and Nanotechnology 2, 475 (2004).
- [6] Shogo Takagi, Naoto Matsuo, Kazushige Yamana, Akira Heya, Tadao Takada, Kenji Sakamoto, Shin Yokoyama, In Proc. 71th Autumn Meeting of The Jpn. Soc. Appl. Phys. 16a-R-9 (2010).
- [7] K. Yamana et al, to be submitted.