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CMOS Op-amp Offset Calibration Technique Using a Closed Loop Offset Amplifier and Compact Resistor String DAC

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I. Introduction

A serious and inherent problem in CMOS op-amps is that their input offset voltage. Demand for a reduction of the input offset voltage of CMOS op-amps grows increasingly with the progress in lowering the supply voltage. To solve this problem, a chopper stabilized amplifier technique is used [1][2]. Since this performs offset correction using switching operations with the internal clock, its use is limited to within the low-frequency range. In addition, there are clock noise problems due to switching. Among other methods for reducing the input offset voltage is that of adjusting with an external resistance [3][4]. These methods require external terminals and adjustment parts. Furthermore, an offset calibration op-amp with feedback control has been proposed that corrects the output voltage by shorting 2 inputs of the op-amp [5][6].

II. Offset Calibration Opamp Architecture

Fig.1(a) shows a block diagram of the conventional offset calibration op-amp. While a conventional system can detect offsets of a microvolts since it has an open loop configuration, it has limitations such as being slow and vulnerable to external noise. Fig.1(b) shows a block diagram of our proposed scheme. The dotted area in Fig.1(b) is an offset amplifier circuit with a closed loop configuration, and the input offset voltage is amplified by about 200 (R_f/R_i=40kΩ/200Ω=200) during the calibration operation. Since the speed of offset amplification is improved by a closed loop operation as shown in Fig.2, the calibration clock cycle can be reduced to approximately one-tenth of that of the open loop configuration. The offset detection precision for our scheme is degraded to 100μV, but is still enough for practical use. The op-amp output is connected to a comparator input, which determines the polarity of the offset voltage. The output signal of the comparator is the up-down signal for a 6-bit digital counter. The D/A converter then converts the 6-bit digital signal to an analog correction signal. The op-amp input offset voltage is self-optimized to reduced level by the feedback control of these circuits.

III. Compact Resistor String D/A

For a D/A converter, we developed a new differential output folded-alternated resistor string D/A converter (FARS-DAC). Fig.3(a) shows a conventional 6-bit resistor string D/A converter. This conventional circuit requires 2×2^N switches and 2^N-1 resistors in the case of configuring an N-bit differential output DAC. In the FARS-DAC, the resistance taps on the REFT(Reference Top) and REFB(Reference Bottom) sides are folded in the center. The REFT or REFB is selected by the MSB bits of the input digital data, and the taps on the REFT and REFB sides are configured to alternate with twice the conventional step as shown in Fig.3(b). Table I shows the tap selection rule of the FARS-DAC for input code m. As shown in Table I, the differential outputs are the same as those of the conventional system while the common mode outputs have fluctuations within a range of ±LSB/2. This system uses only the even-numbered taps from the taps numbered 32 or less, and only the odd-numbered taps from the taps numbered 33 or greater, as shown in Table I. Therefore, the total number of switches is $2^{(N-1)}$+5, and the number of switches can be reduced to about one-fourth of the conventional system. In addition a 2R resistor is regarded as the unit resistor, the resistor at the middle (R_{33}) is made by the parallel connection of two 2Rs, and the total number of resistors is reduced to almost half that of a conventional system. Fig.4 shows the offset trimming circuit. The PMOSFETs (PT0, PT1, PT2) in the dotted area are added and their gate widths are one sixth of the PMOSFETs (P0, P1, P2) of the op-amp to be calibrated. Common mode fluctuations in the output voltage of the FARS-DAC are successfully suppressed by a common mode rejection ratio of over 30dB in this circuit.

IV. Test Chip Fabrication and Measurement Results

A test chip is fabricated using the TSMC-0.35um standard CMOS process. Fig.5 shows the relationship between the offset correction data and the offset voltage. The output of the FAR-DAC has a 5mV step and we confirmed the correction step of 0.85mV (=5mV/6) experimentally. Fig.6 shows the offset voltage distributions before and after calibration. The offset voltage is successfully curbed to ±1.5mV or less by calibration. The average offset voltage after calibration is about -0.3mV, which would be an error attributable to the offset of the comparator circuit itself. Table II is a summary of the overheads of our offset calibration op-amp. The increment of power consumption due to the calibration circuit is small at approximately 70μA. Fig.7 shows a layout of the op amp area and the FARS-DAC. The area of the differential output the FARS-DAC is 0.013mm^2.

V. Conclusions

We have presented a high-speed and compact offset calibration circuit technique for an op-amp that can be applied after production. With this technology, the miniaturization of a whole op-amp system can be achieved, because the layout size of each circuit consisting of op-

amps can be reduced by performing offset correction.

ACKNOWLEDEMENTS

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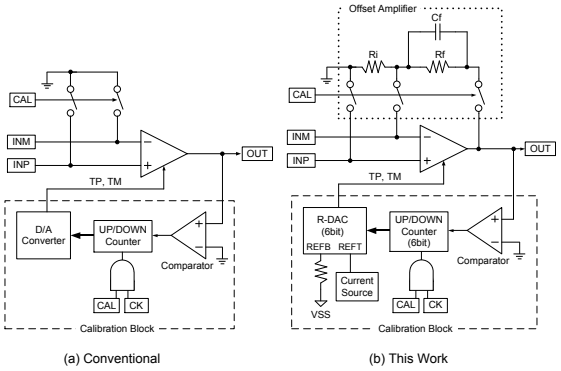

Fig. 1 Block diagram

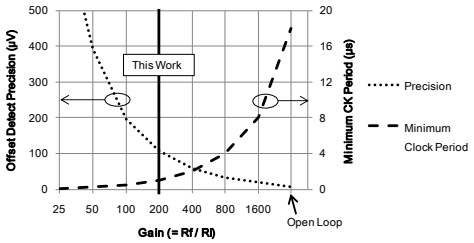

Fig. 2 Offset detect precision vs. Clock period

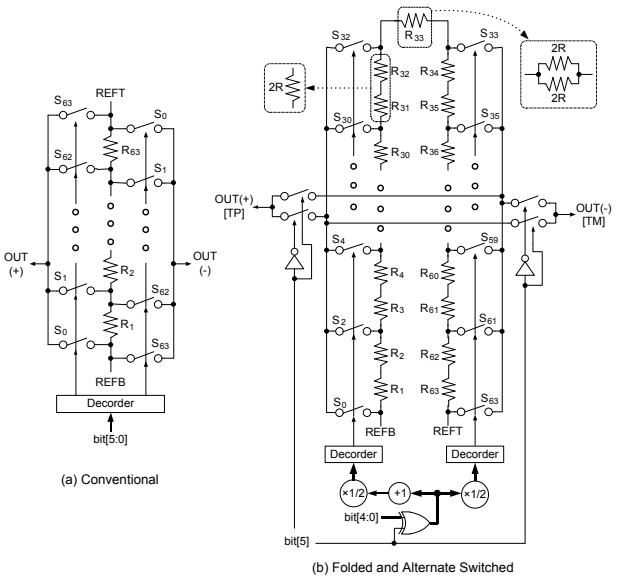

Fig. 3 Resistor string D/A Converter (6bit)

Table I Output tap table for Input codes

Code =m	Conventional				This Work			
	Tap (+)	Tap (-)	Diff	Com	Tap (+)	Tap (-)	Diff	Com
0	0	63	-63	31.5	0	63	-63	31.5
1	1	62	-61	31.5	2	63	-61	32.5
2	2	61	-59	31.5	2	61	-59	31.5
3	3	60	-57	31.5	4	61	-57	32.5
30	30	33	-3	31.5	30	33	-3	31.5
31	31	32	-1	31.5	32	33	-1	32.5
32	32	31	1	31.5	33	32	1	32.5
33	33	30	3	31.5	33	30	3	31.5
61	61	2	59	31.5	61	2	59	31.5
62	62	1	61	31.5	63	2	61	32.5
63	63	0	63	31.5	63	0	63	31.5

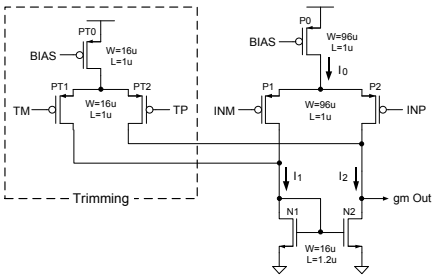

Fig. 4 Offset trimming circuit

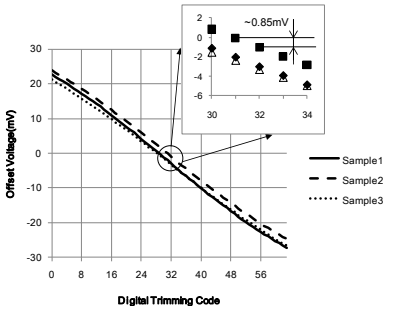

Fig. 5 Offset voltage vs. Digital trimming code

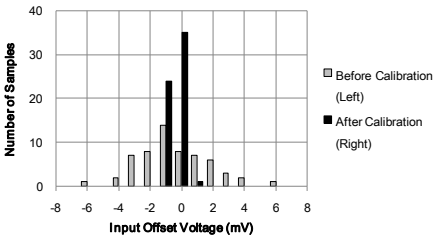

Fig. 6 Offset voltage histogram

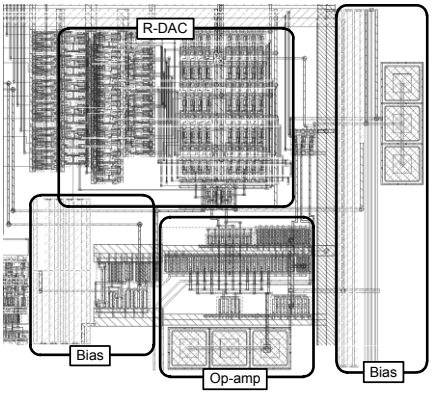

Fig. 7 Op-amp and R-DAC layout

Table II Current and Area of Blocks

Block Name	Current(mA)	Area(mm2)
Op-amp	1.03	0.007
Bias	0.24	0.016
FAR-DAC	0.04	0.013